CINEMATRONICS INC.

SERVICE MANUAL

CPU EXORCISOR MANUAL

CINEMATRONICS INC.

INTRODUCTION

The Exorciser Test Fixture is a diagnostic tool designed to be used in conjunction with a signature analyzer to trouble shoot the main logic board of a Cinematronics game.

A signature analyzer is a piece of test equipment which is used to monitor digital signals versus time, and which produces an alphanumeric readout which represents the signal's "signature". Any circuit can be tested by measuring the signatures of the desired signals and then comparing them to previously determined correct signatures.

The purpose of the Exorciser circuit is to provide a known set of reference inputs to the logic board. These reference inputs are designed to generated a known set of signatures which the signature analyzer can them measure. When the two dip headers in positions U14 and D8, containing the jumper wites are removed from the logic board, various signal paths are disconnected. Inserting the Exprciser cables into these sockets allows the Exorciser to inject it's reference signals into the main logic board. The actual Exorciser circuit consists of a 16-bit counter chain whose outputs are then combined via a number of simple gating circuits to generate the input reference signals. There is also circuitry to produce the start/stop signal to the signature analyzer.

CONNECTING THE EXORCISER TO THE LOGIC BOARD

Connect a regulated +5V supply to the exerciser inputs and the logic board. Remove dip jumper U14 and insert the header of the center cable, J1. Remove jumper D8 and insert the header of cable J3. Attach "E-Z" hooks to ground pins of nearest IC.

Next attach the 3 chip clips at the end of Exorciser connector J2. Place the clip with the red dot facing the logic board on the Ic at position T2. Attach the blue dotted clip to position R2 and

the yellow dotted clip to position N2. Ground the test point located to the left of U2. This must always be done when the clips are attached.

CONNECTING THE EXORCISER TO THE SIGNATURE ANALYZER

Connections from the signature analyzer to the Exorciser are straight forward. Both the start and stop leads on the signature analyzer connect to the test point labeled start/stop on the Exorciser front panel. Also connect the clock and ground leads from the analyzer to their respective test points on the Exorciser.

The spare clock terminal on the front panel should be connected to the clock test point on the logic board located between J4 and K4. This can easily be done with a cable terminated at both ends with E-Z hooks.

SIGNATURE ANALYZER OPERATING MODE

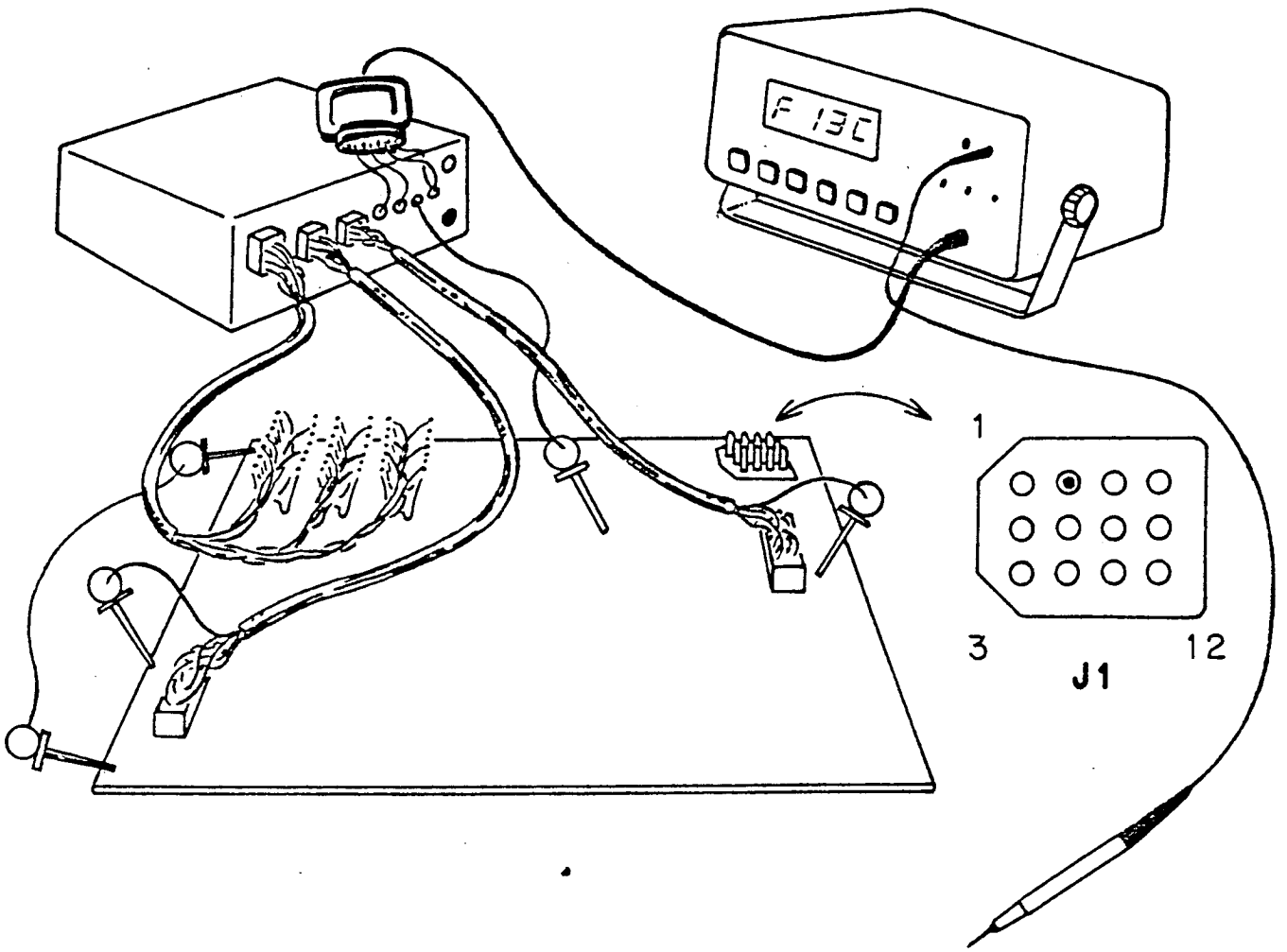
To achieve the proper signatures the signature analyzer must be set up to trigger on the proper pulse edge. Both the start and clock trigger on the trailing edge. The stop triggers on the leading edge.

NOTE: On Space Wars and Tailgunner a jumper wire must be installed from A8, Pin 8 to T2, Pin 4 on the main logic board. Once installed, leave it in place permanently as it will not affect Space Wars normal operation. Remove from Tailgunner after repair.

Also, a temporary jumper grounding TP8 which is located in the upper left corner above U2 should be installed. Remove this jumper after repair.

OPERATING INSTRUCTIONS

Once all the set up connections are made and power applied, check C8 Pin 12 for the signature U6HH. If this signature is unstable then recheck all the connections, especially the 3 16 pin clips. When stability is acheived, check the signatures at C8 Pins 5 and 6. They should be C32P. If they are not, recheck the connections at D-8. The header may have been installed improperly.

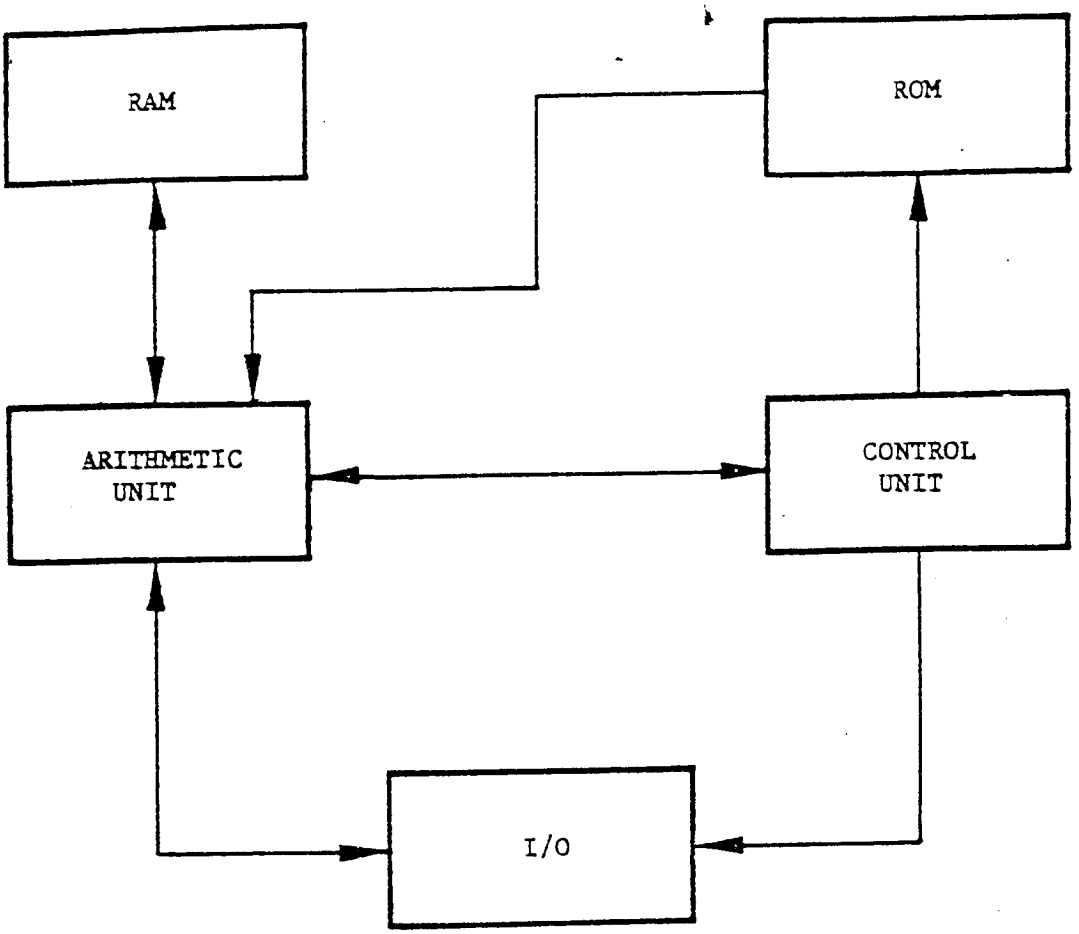

F 13C
1
3
12
J1

Trouble shooting the electronics on the main logic board with the Exorciser and signature analyzer should be done in the same manner as when using an oscilliscope. When a bad output is encountered, one shold first investigate the control lines before assuming that the particular I.C. is bad. If one or more inputs are incorrect, continue back tracking until the problem is isolated to a bad output with good inputs. The problem would then be confined to either the I.C. with the bad output or to any I.C. it connects to.

CPU TROUBLESHOOTING GUIDE

This section describes the various blocks of the main logic board and lists a few quick check points for each block. Should a logic board pass these checks, verigy that the remaining signatures on the signature schematics are correct. Remember: This is a "patience" procedure - if a board is bad there exists a bad signature somewhere.

The main logic board can be diagrammed as follows:



Functional Block Diagram

CPU QUICK & DIRTY TROUBLESHOOTING GUIDE

LOCATION	TYPE	PIN#	SIG.	PAGE A	PAGE F	INSTRUCTION	IN/OUT	FROM/TO A	FROM/TO F
F-14	74LS287	9	1846	4	5	$\overline{LDR}$	out	4	5
		10	FP05	4	5	$\overline{LIR}$	out	4	5
		11	8399	4	5	$\overline{ACC}$	out	4	5
		12	61C3	4	5	ADV	out	4	5
F-2	74LS259	1	PH07	1	1	D_0	in	3	4
		2	29A9	1	1	D_1	in	3	4
		3	80HP	1	1	D_2	in	3	4
N-9	74LS85	5	A197	2	3	ACC	out	4	5
		6	237P	2	3	=ACC	out	4	5
L-4	74LS182	9	AH4H	2	3	$\overline{Carry}$	out	4	5
L-2	74LA10	4	F1CH	2	2	ACC	in	4	5
J-6	74LS10	8	F12C	2	2		out	2	2
C-6	74LS163	15	0109	5	6	Line Done	out	5	6
J-2	74LS32	3	9820	5	6	Intensity	out	7406	
		11	2873	5	6	Bright	out	7406	
H-8	74LS02	13	U97A	5	6	Initial Position	out	LF	
I-8	74LS04	2	204A	5	6	Line Drawing	out	LF	
A-12	74LS32	3	390P/2AF1	4	5	$\overline{LPA}$	out	3	4
H-14	74S02	10	HOU8/07U2	3	4	System/Ready	out	3	4
U-7	P_ROM	1	C443 4473	3	4	A_7	in	3	4
		2	FC92 FA45	3	4	A_6	in	3	4
		3	5PF4 FF86	3	4	A_5	in	3	4
		4	A7U5 H162	3	4	A_4	in	3	4
		5	UPAP 0A1F	3	4	A_3	in	3	4
		6	HAOO UUF5	3	4	A_2	in	3	4
		7	8066 1285	3	4	A_1	in	3	4
		8	7211 U801	3	4	A_0	in	3	4
		23	U62F 3124	3	4	A_9	in	3	4
		22	0499 A8PF	3	4	A_{10}	in	3	4
		19	578F 4U1H	3	4	A_{11}	in	3	4
		18	473U	3	4	$\overline{PG}$ Flop	in	3	4
H-12	74LS194	15	7H33	2	3		out	2	3
		14	H255	2	3		out	2	3
		13	54CC	2	3	PG_1	out	2	3
		12	OPH1	2	3	PG_0	out	2	3
J-12	74LS298	10	AAP8	2	3	INDR	in	4	5
L-14	2102	20	4A50	2	3	R/W	in	4	5

LOCATION	TYPE	PIN#	SIG.	PAGE A	PAGE F	INSTRUCTION	IN/OUT	FROM/TO A	FROM/TO F
M-14	2102	20	4A50	2	3	R/W	in	4	5
N-14	2102	20	4A50	2	3	R/W	in	4	5
U-9	74LS75	4,13	H33C	3	4		in	3	4
U-11	74LS157	1	90AP	3	4		in	3	4
		15	C32P	3	4	Reset	in		

CONTROL SECTION (SHT 5 of 7)

This section decodes instructions (I0-I7) from memory to various control lines necessary for the rest of the computer. Verify correct signatures at the following points:

LOCATION	TYPE	PIN #	SIGNATURE
F14	74LS287	9	1846
		10	FP05
		11	8399
		12	613C
E14	74LS288	1	OC45
		2	320U
		3	C530
		4	1PO2
		5	394A
		6	8PP6
		7	409C
		9	07PU
D14	74LS288	1	2H8F
		2	A76P
		3	41UC
		4	7P23
		5	9A6A
		6	5H61
		7	8ACC
		9	5AA5
C14	74LS288	1	9069
		2	7323
		3	CH9A
		4	96UA
		5	67AH
		6	2PFF
		7	32U4
		9	U100

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LOCATION	TYPE	PIN#	SIGNATURE
D10	74LS02	1	7341
B12	74LS10	6	077H
A10	74LS00	6	7890
		11	802H
		3	6PF3
C8	74LS107	5	C32P
B8	74LS107	2	4A50
A8	74LS107	2	49P2
B12	74LS10	12	FICH*
B6	74LS04	2	Logic High
A12	74LS32	3	390P/2AF1

*If bad, check F6-6 is 6598, F6-6 bad, see "Load Timer Loop" in following section.

ARITHMETIC SECTION (SHT 2 of 7, SHT 3 of 7)

Most mathematical manipulations are performed in this section. The "X" and "Y" accumulators, ALU's and scratchpad memory (RAM) are contained on these sheets.

LOCATION	TYPE	PIN#	SIGNATURE
L4	74S182	9	AH4H
L6	25LS181	9	9115
		10	61CA
		11	91CA
		13	6121
M6	25LS181	9	F43F
		10	5000
		11	34CP
		13	66UU
N6	25LS181	4	1C14
		10	8236
		11	304P
		13	FC6A
N9	74LS85	5	A197
		6	237P
L14	9101C	20	4A50
M14	9101C	20	4A50

LOCATION	TYPE	PIN#	SIGNATURE
N14	9101C	20	4A50
J12	74LS298	10	AAP8
*I12	74LS298	15	0038
	*GND pin 10 for this test	14	6034
		13	UCCC
		12	PF3C
*J12	*74LS298	15	PPC3
	GND pin 10 for this test	14	01F4
		13	4024
		12	F6C6
M4	74LS194	15	AC5H
		14	242C
		13	0841
		12	0U1F
P4	74LS194	15	725C
		14	FUC5
		13	30CC
		12	P38A
S4	74LS194	15	725C
		14	FUC5
		13	30CC
		12	P38A
N4	74LS194	15	C432
		14	166U
		13	67HU
		12	26PP
R4	74LS194	15	HAC9
		14	FPF2
		13	711H
		12	9172
T4	74LS194	15	F567
		14	651H
		13	UAC3
		12	HAFA

ROM (Game Memory)

Inside the ROM's are the instructions, data, and addresses for the particulat game. Cinematronics games have an 8K memory capacity divided between an even 4K ROM and odd 4K ROM.

LOCATION	TYPE	PIN #	SIGNATURE
U7,R7,T7,P7	ROM	1	C443
		2	FC92
		3	5PF5
		4	A7U5
		5	UPAP
		6	HA00
		7	8066
		8	7211
		23	U62F
		22	0499
		19	578F
		18	473U (Logic High on s/w and S.H.)
U11			
T11			
U9	see No-Op test for particular game		
T9			
H14	74S02	10	07U2
		4	0000
			H33C * Reverse Clock Position
J14	74S288	1	H666
		2	FU3U
		3	P503
		4	C15P

I/O SECTION (SHTS 6 and 1)

These are the channels by which the conputer receives information from the player controls and sends proper control signals to the monitor and audio board. (Note: It is best to measure output signals at the particular connector that they exit the board.

The pin number and connector designation is included in parenthesis).

LOCATION	TYPE	PIN#	SIGNATURE
M2	74LS377	9 (J2-1)	PP4F
		19 (J2-2)	LO
		2 (J2-3)	LO
		6 (J2-4)	C7P5
P2	74LS377	9 (J2-5)	C7P5
		19 (J2-6)	AA58
		2 (J2-7)	2ACF
		6 (J2-8)	1H2A
S2	74LS377	9 (J2-9)	U366
		19 (J2-10)	1H2A
		2 (J2-11)	3796
		6 (J2-13)	3796
M2	74LS377	16 (J2-21)	LO
		12 (J2-23)	8A2A
		15 (J2-25)	6P3U
		5 (J2-26)	8A2A
P2	74LS377	16 (J2-27)	6P3U
		12 (J2-28)	P415
		15 (J2-29)	LO
		5 (J2-30)	6P3U
S2	74LS377	16 (J2-31)	6P3U
		12 (J2-32)	8A2A
		15 (J2-33)	6P3U
		5 (J2-34)	6P3U
J2	74LS32	3 (J2-12)	9820
		11 (J2-14)	2873
H8	74LS32	13 (J2-18)	U97A
		11 (J2-19)	204A
A6	74LS02	10	9069
F2	74LS259	4	FH1H
		5	54P5
		6	8CAU
		7	2043

LOCATION	TYPE	PIN#	SIGNATURE
		9	A941
		10	A328
		11	C9UC
		12	82CU
VERIFY WITH SCOPE			
F4	74LS10	6	
J4	74265	6	5 MHZ Clock
		7	$\overline{5 \text{ MHZ Clock}}$
		9	5 MHZ Clock
		10	$\overline{5 \text{ MHZ Clock}}$

NO OP TEST

Because of the nature of the CPU exorciser the program ROMS and chips U9, T9, U11 and T11 are not tested. To test the proper operation of these chips the No-Op test is used.

(a) Tie pins 11 and 15 of a 16 pin header to a common E-Z hook. Place header in socket U14 and connect E-Z hook to Ground. This grounds pins 11 and 15 of socket. Connect start and stop lines of signature analyser to reset test point on CPU board below IC T11. Connect Clok of signature analyser to clock on CPU.

You are now ready to conduct the No-Op test.

SPAC TEST

The SPAC test is used because the standard exorciser test removes chips N2, R2 and T2 from the accumulator loop.

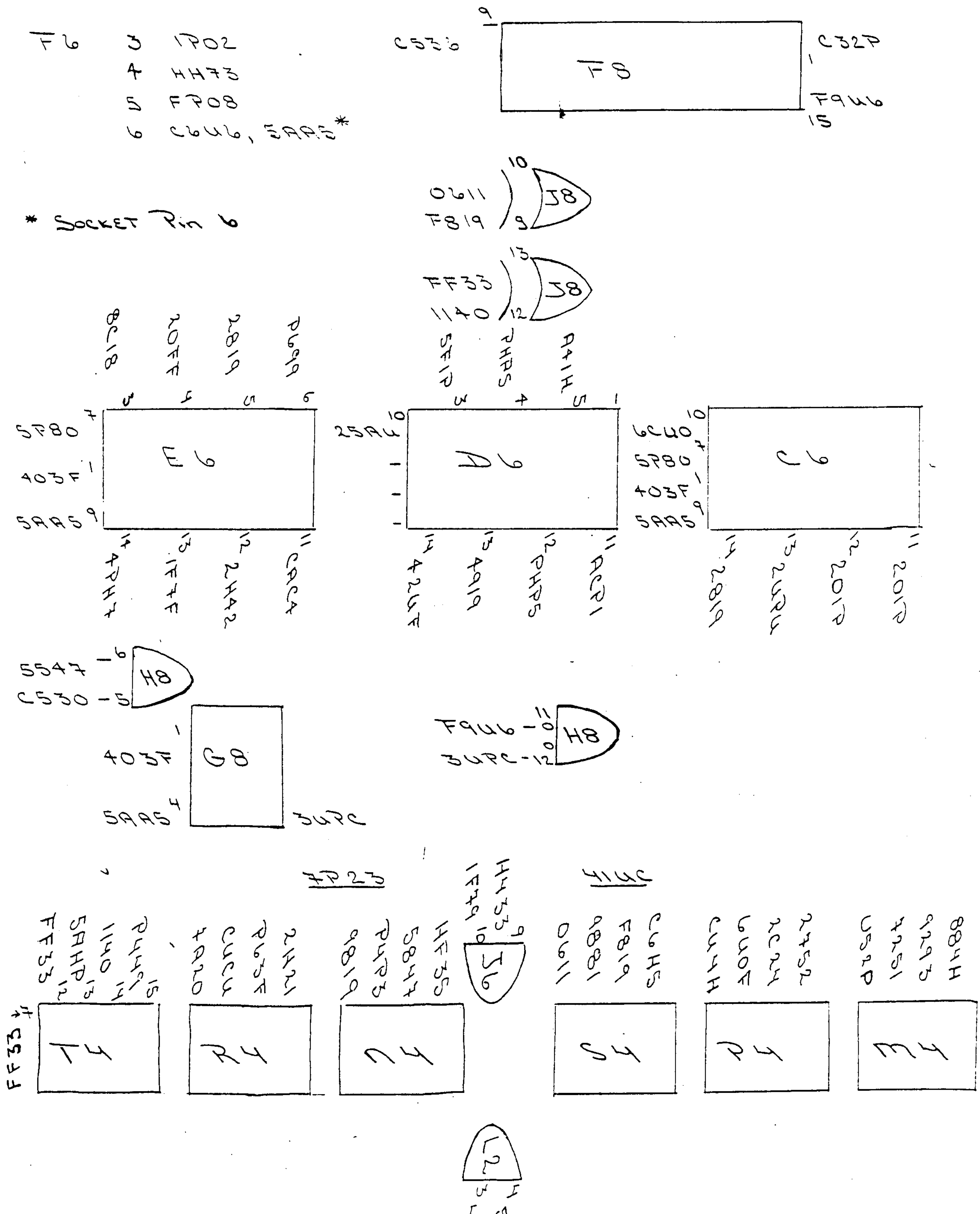
To conduct the SPAC test set up the exorciser as per instructions in manual with the following exceptions:

(a) DO NOT connect jumper from ground to test point #8.

(b) DO NOT connect dip clips to chips T2, R2 and N2.

LOAD TIMER LOOP TEST

This test allows you to test the accumulator section of the



Load Timer Loop Test

CPU board. It is done in the following manner:

(a) Set up exorciser as per instructions in manual.

(b) Remove IC F6 pin 6 from socket.

(c) Connect IC F6 pin 13 to socket F6 pin 6.

Load timer loop test may now be run.

EXORCISER OUTPUTS

	T-2	R-2	N-2
4)	615F	A69C	F469
7)	A928	47F6	PH6F
9)	A29F	8CC5	211U
12)	96FC	510F	H28U

	U-14		D-8
16)	HC89	4)	7825
15)	52F8	5)	655C
14)	UPFH	16)	U6HH
13)	OAFA	15)	H1
12)	5H21	14)	2518
11)	7F7F	11)	8UC2
10)	CCCC	10)	6PF3
9)	5555	9)	802H

SPAC TEST

	T-2	R-2	N-2
4)	3605	3488	6784
7)	5U25	3U40	7525
9)	7U7A	50A3	5938
12)	323C	0708	P19C

OUTPUTS J-2

1)	PP4F	2)	LO
3)	LO	4)	C7P5
5)	C7PF	6)	AA58
7)	2ACF	8)	1H2A
9)	U366	10)	1H2A
11)	3596	12)	9820
13)	3796	14)	2873/C9UC
15)	LO	16)	unstable
17)	LO	18)	U97A
19)	204A	20)	LO
21)	LO	22)	LO
23)	8A2A	24)	LO
25)	6P3U	26)	8A2A
27)	6P3U	28)	P415
29)	LO	30)	6P3U
31)	6P3U	32)	8A2A
33)	6P3U	34)	6P3U

OUTPUTS J-4

		10)	Float
11)	FHIF	12)	54P5
13)	8CAU	14)	2043
15)	A941	16)	82CU

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NO OPP U-14

	Space	Star	Sun	Tail	Rip
1)	306A	FHIF	A332	6P7F	1886/PC3H
2)	0222	2P35	HH07	UH3C	1602/2206
3)	4P55	5FH8	P13U	AUFH	C4PH/HU31
4)	51C1	6UPH	82P1	81UP	C1A7/6PP7
5)	3A7C	2P27	81U5	37C8	42U4/OP7A
6)	A315	75HH	5FF2	9F5H	6A7F/P193
7)	742A	20AU	6F01	17A8	9995/F019
8)	6H96	6200	FH4F	3FP7	522H/0U90

RIP OFF

Analyzer setting- clock in or out to obtain stable signature

U-11

1)	UUUU	16)	Vcc
2)	Unstable/C7A2	15)	Lo/pulsing 0000
3)	857C/P198	14)	unstable/CA92
4)	9995/F019	13)	2U1U/494C
5)	unstable	12)	1886/PC3H
6)	9P4H/1A61	11)	unstable
7)	42U4/OP7A	10)	U478/H53P
8)	Gnd	9)	C4PH/HU31

U-9

1)	8578/P199	16)	857C/P198
2)	unstable/H186	15)	9P4H/1A61
3)	unstable/PC6H	14)	9P4F/1A60
4)	UUUP	13)	UUUP
5)	Vcc	12)	Gnd
6)	unstable/1A84	11)	U479/H53U
7)	unstable/5P6F	10)	U478/H53P
8)	2U1P/494A	9)	2U1U/494C

NO-OP SIGNATURES

T-11

1)	UUUU	16)	Vcc
2)	unstable/1PF2	15)	Lo/0000 Pulsing
3)	7C1A/5AF1	14)	unstable
4)	1602/2206	13)	976H/H287
5)	unstable/7H3P	12)	532H/0U90
6)	4148/9022	11)	unstable
7)	C1A7/6PP7	10)	F58C/C66F
8)	Gnd	9)	6A7F/P193

U-14

1)	1886/PC3H
2)	1602/2206
3)	C4PH/HU31
4)	C1A7/6PP7
5)	42U4/OP7A
6)	6A7F/P193
7)	9995/F019
8)	532H/0U90

continued next page

T-9

1)	7C1C/5AF0	16)	7C1A/5AF1
2)	Unstable	15)	4148/9022
3)	Unstable/ OC6F	14)	4149/9023
4)	UUUP	13)	UUUP
5)	Vcc	12)	Gnd
6)	Unstable/ 6A84	11)	F58A/C66H
7)	Unstable/ A01U	10)	F58C/C66F
8)	976F/H286	9)	976H/H287

U-7, T-7, R-7, P-7

1)	7791	24)	Vcc
2)	6F9A	23)	6321
3)	U759	22)	37C5
4)	0356	21)	Vcc
5)	1U5P	20)	Lo
6)	P763	19)	6U28
7)	8484	18)	Hi
8)	FFFF	17)	Unstable
9)	Unstable	16)	Unstable
10)	Unstable	15)	Unstable
11)	Unstable	14)	Unstable
12)	Gnd	13)	Unstable

TAILGUNNER

NO-OP SIGNATURES

Analyzer setting- clock in or out to obtain stable signature.

U-11

1) UUUU	16) Vcc
2) 25F5	15) Lo
3) 36C6	14) 01P1
4) 17A8	13) H66C
5) UH13	12) 6P7F
6) U6P0	11) 36A0
7) 37C8	10) A64A
8) Gnd	9) AUFH

T-11

1) UUUU	16) Vcc
2) unstable	15) Lo
3) HUCH	14) 38AP
4) UH3C	13) 3FP7
5) unstable	12) 3FP7
6) 83H5	11) unstable
7) 81UP	10) 4F2H
8) Gnd	9) 9F9H

U-14

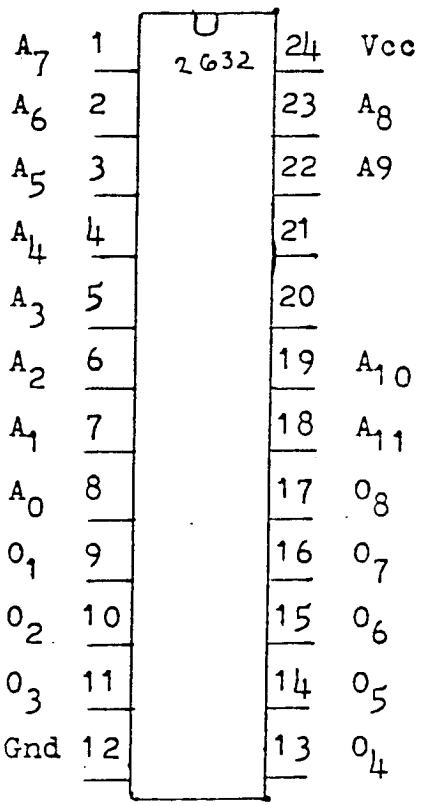
1) 6P7F	
2) UH3C	
3) AUFH	
4) 81UP	
5) 37C8	
6) 9F9H	
7) 17A8	
8) 3FP7	

U-9

1) 36C7	16) 36C6
2) 7073	15) U6P0
3) 0068	14) U6P1
4) UUUP	13) UUUP
5) Vcc	12) Gnd
6) unstable	11) A64C
7) unstable	10) A64A
8) H66A	9) HCC6

T-9

1) HUCF	16) HUCH
2) P7F6	15) 83H5
3) 07AC	14) 83H4
4) UUUP	13) UUUP
5) Vcc	12) Gnd
6) unstable	11) 4F2F
7) unstable	10) 4F2H
8) 38A8	9) 38A9



T-7

1) 7791	24) Vcc
2) 6F9A	23) 6321
3) U759	22) 37C8
4) 0356	21) Lo
5) 1U5P	20) Lo
6) P763	19) 6U28
7) 8484	18) Lo
8) FFFF	17) H6PH
9) 01P1	16) unstable
10) C17P	15) H02H
11) 65F8	14) 4F6P
12) Gnd	13) 25F5

R-7

1) 7791	24) Vcc
2) 6F9A	23) 6321
3) U759	22) 37C8
4) 0356	21) Lo
5) 1U5P	20) Lo
6) P763	19) 6U28
7) 8484	18) Lo
8) FFFF	17) P7F6
9) unstable	16) 07AC
10) unstable	15) unstable
11) 0068	14) unstable
12) Gnd	13) 7037

STAR HAWK

NO-OP SIGNATURES

Analyzer setting- clock in or out to obtain stable signature.

U-11

1) UUUU	16) Vcc
2) 3P03	15) Lo
3) FHU0	14) 8FA5
4) 20AU	13) 87AA
5) 88AH	12) FH1F
6) 6C87	11) H345
7) 2P27	10) A3A1
8) Gnd	9) 5FH8

T-11

1) UUUU	16) Vcc
2) 2536	15) Lo
3) 1429	14) 3316
4) 2P35	13) P3HH
5) F859	12) 6200
6) 9705	11) 5FA0
7) 6UPH	10) FHF5
8) Gnd	9) 75HH

U-14

1) FH1F	
2) 2P35	
3) 5FH8	
4) 6UPH	
5) 2P27	
6) 75HH	
7) 20AU	
8) 6200	

U-9

1) FHU1	16) FHU0
2) unstable	15) 6C87
3) unstable	14) 6C86
4) UUUP	13) UUUP
5) Vcc	12) Gnd
6) unstable	11) A3A0
7) unstable	10) A3A1
8) 87AC	9) 87AA

T-9

1) 1428	16) 1429
2) 1HF9	15) 97P5
3) unstable	14) 97P4
4) UUUP	13) UUUP
5) Vcc	12) Gnd
6) unstable	11) FHF4
7) unstable	10) FHF5
8) P3HF	9) P3HH

U-7

1) 7791	24) Vcc
2) 6F9A	23) 6321
3) U759	22) 37C5
4) 0356	21) Lo
5) 1U5P	20) Lo
6) P763	19) 6U28
7) 8484	18) Hi
8) FFFF	17) 2536
9) 8FA5	16) F859
10) H345	15) 5FA0
11) 88AH	14) 3316
12) Gnd	13) 3P03

U-7

1) 7791	24) Vcc
2) 6F9A	23) 6321
3) U759	22) 37C5
4) 0356	21) Lo
5) 1U5P	20) Lo
6) P763	19) 6U28
7) 8484	18) Hi
8) FFFF	17) unstable
9) unstable	16) unstable
10) unstable	15) unstable
11) unstable	14) unstable
12) Gnd	13) unstable

SPACE WARS

NO-OP SIGNATURES

Analyzer setting- clock in or out to obtain stable signature.

U-11

1)	UUUU	16)	Vcc
2)	unstable	15)	Lo
3)	818H	14)	unstable
4)	742A	13)	5815
5)	unstable	12)	306A
6)	HH22	11)	0U87
7)	3A7C	10)	73PF
8)	Gnd	9)	4P55

T-11

1)	UUUU	16)	Vcc
2)	unstable	15)	Lo
3)	A9UF	14)	C541
4)	0222	13)	9762
5)	unstable	12)	6H96
6)	2571	11)	unstable
7)	51C1	10)	6A94
8)	Gnd	9)	A315

U-14

1)	306A		
2)	0222		
3)	4P55		
4)	51C1		
5)	3A7C		
6)	A315		
7)	742A		
8)	6H96		

U-9

1)	818F	16)	818H
2)	unstable	15)	HH22
3)	unstable	14)	HH23
4)	UUUP	13)	UUUP
5)	Hi	12)	Gnd
6)	unstable	11)	739H
7)	unstable	10)	739F
8)	5814	9)	5815

T-9

1)	A9UH	16)	A9UF
2)	unstable	15)	2571
3)	unstable	14)	2570
4)	UUUP	13)	UUUP
5)	Hi	12)	Gnd
6)	unstable	11)	6A94
7)	unstable	10)	6A94
8)	9763	9)	9762

U-7

1)	7791	24)	Vcc
2)	6F9A	23)	6321
3)	U759	22)	37C5
4)	0356	21)	Lo
5)	1U5P	20)	Lo
6)	P763	19)	6U28
7)	8484	18)	Hi
8)	FFFF	17)	unstable
9)	unstable	16)	1516
10)	0U87	15)	unstable
11)	unstable	14)	C541
12)	Gnd	13)	unstable

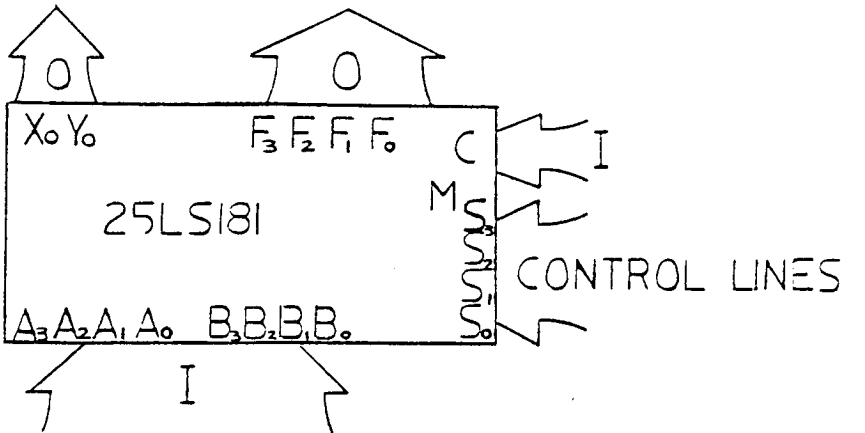
R-7

1)	7791	24)	Vcc
2)	6F9A	23)	6321
3)	U759	22)	37C5
4)	0356	21)	Lo
5)	1U5P	20)	Lo
6)	P763	19)	6U28
7)	8484	18)	Hi
8)	FFFF	17)	unstable
9)	unstable	16)	unstable
10)	unstable	15)	unstable
11)	unstable	14)	unstable
12)	Gnd	13)	unstable

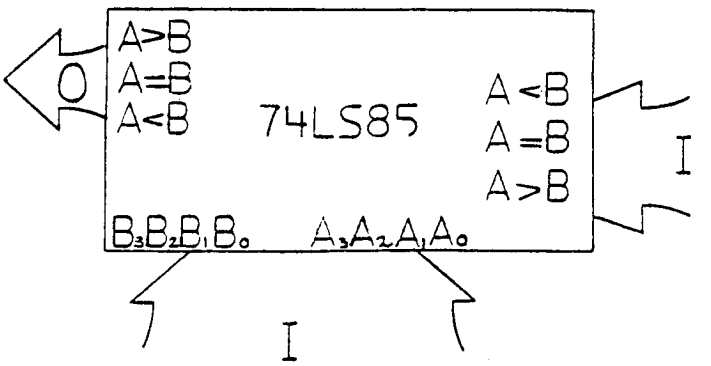
FLOW CONCEPTS

For signature analysis purposes, one need only know the flow of the system under test. This section reveals the flow, (inputs, outputs, and control lines) of the major IC's used on Cinematronics logic boards.

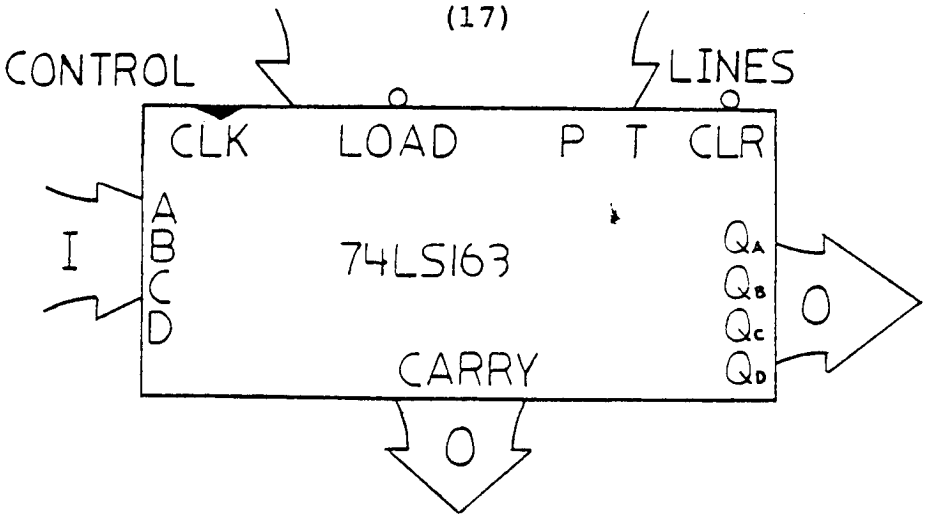
Keep in mind that bad control lines are more significant than bad inputs, so that when an output of a particular IC is suspected as faulty, check control lines first.



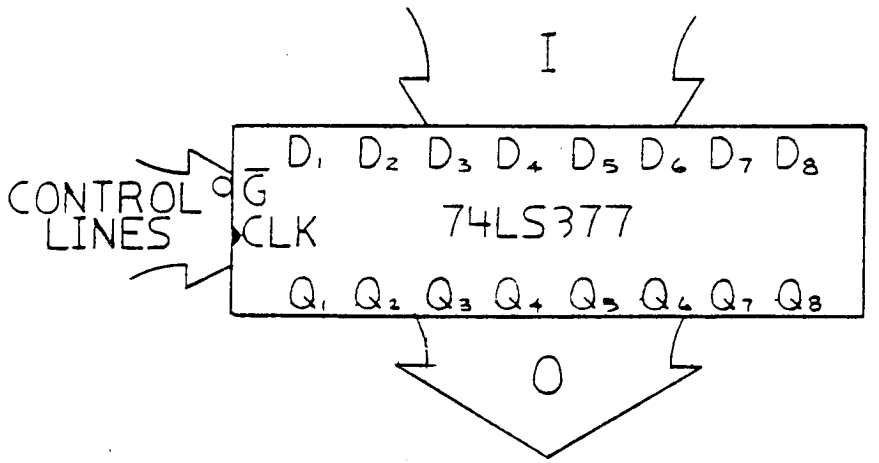
The arithmetic logic unit (ALU) performs 16 different arithmetic and logic operations (based on the control line combinations) on two four-bit words: A0-A3 and B0-B3. The result is transmitted to the function outputs F0-F3.



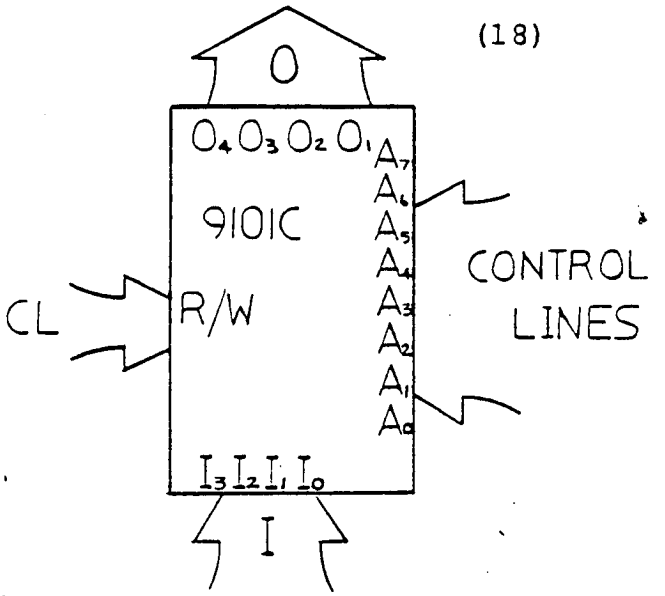
These four bit magnitude comparators generate three status lines that indicate whether the "A" word (A0-A3) is less than, equal to, or greater than the "B" input word (B0-B3).



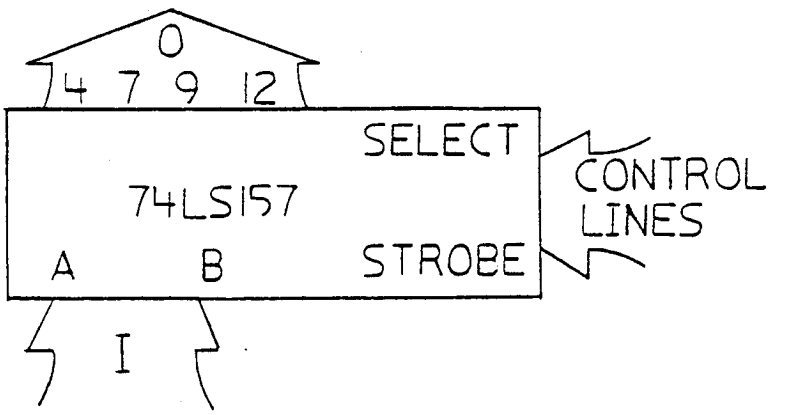
These IC's are four-bit binary counters. The input word can be transferred directly to the output and the counting procedure may start from this preset value, or the outputs can be cleared to start counting from zero.



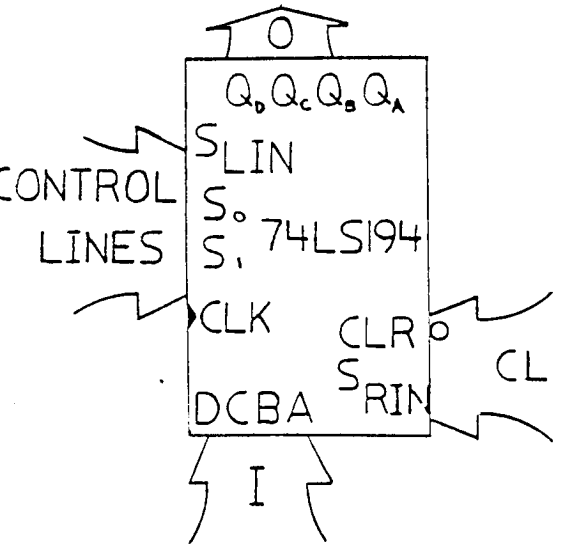
These devices are eight bit data latches. When the proper control lines are active, the data present on the inputs is latched to the outputs.



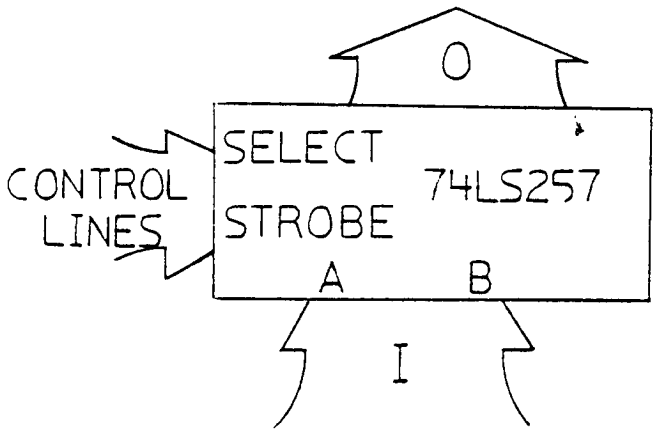
The 9101 is a random access memory (RAM) used for storing variables, data, and intermediate computational results. The input word is either stored at the address location code (A0-A7) or the word at that location is fed directly to the outputs.



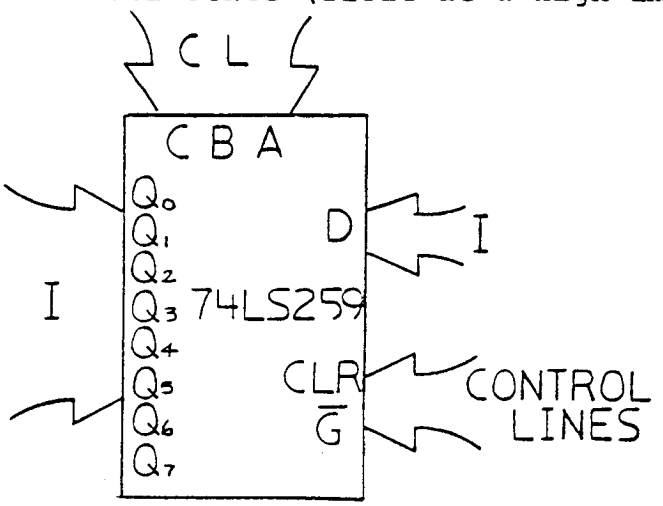
These data selectors channel either four bit word "A" or "B" to the four output channels. The status of the select line determines which word is selected.



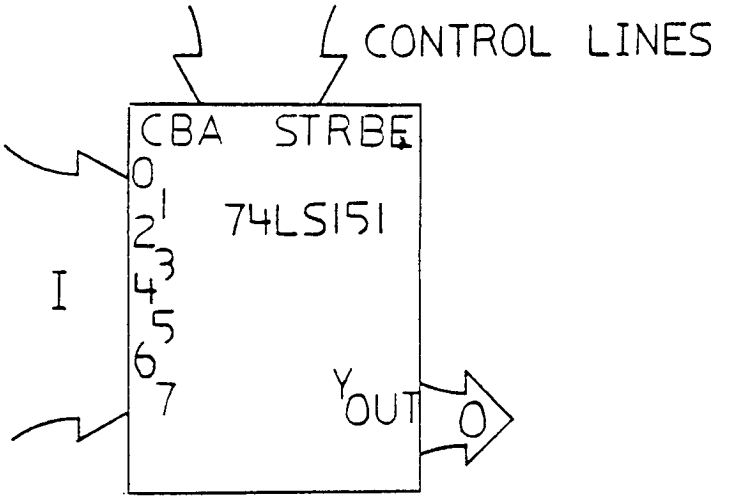
The 74LS194 is a four-bit Bi-directional shift register that does one of four functions to the inputs in response to control lines So and S1: The device either loads the inputs directly to the outputs, shifts left, shifts right, or does nothing.



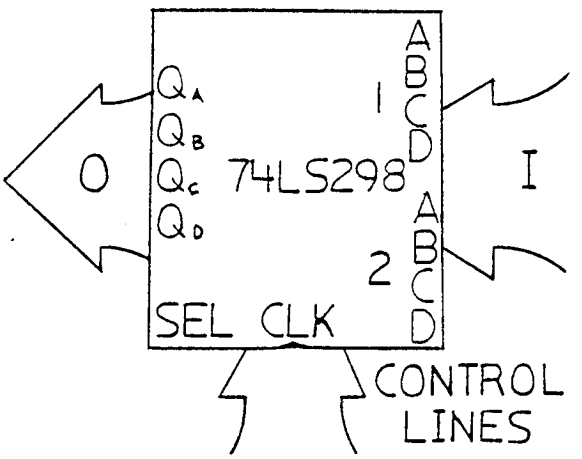
Identical in operation to the 74LS157 but with the strobe line causing the output bits to tri-state (float at a high impedance).



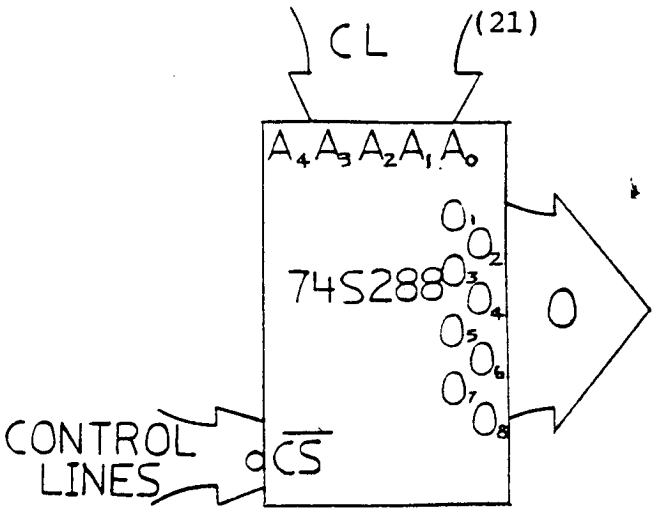
This device receives data at the input and channels it to one of eight outputs based on control lines A, B, and C.



The 151 functions just opposite of the 259. Data present at one of the eight inputs is channeled to the single output. The control lines select the particular input line to be read to the output.



Similar to the 257 with the addition of a synchronous clock line, word "1" or "2" is fed to the output at the next clock pulse depending on the select line state.

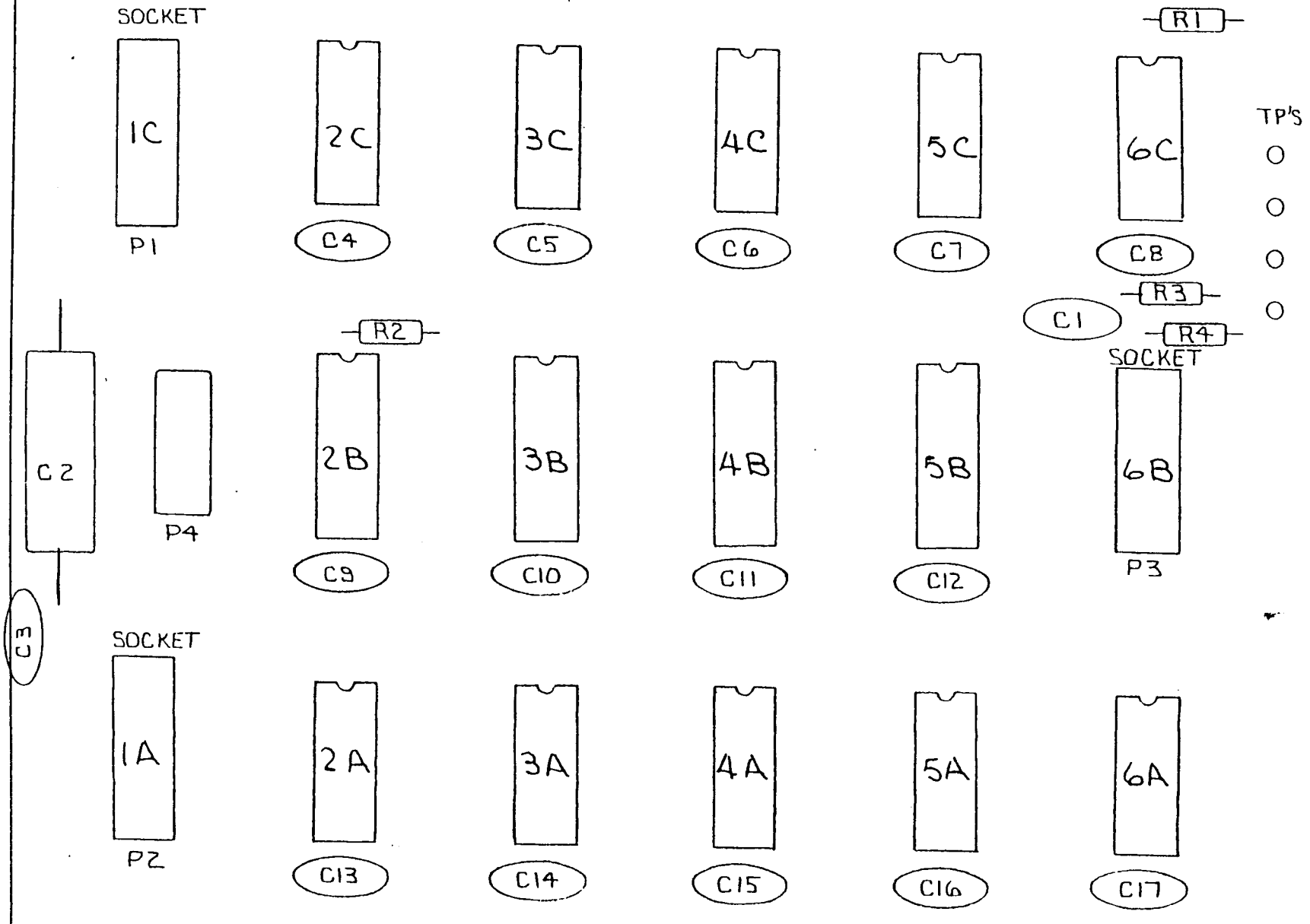


These devices are ROM's (Read Only Memory). The output is an eight-bit digital word that is pre-programmed into the location specified by the address lines (A0-A4)

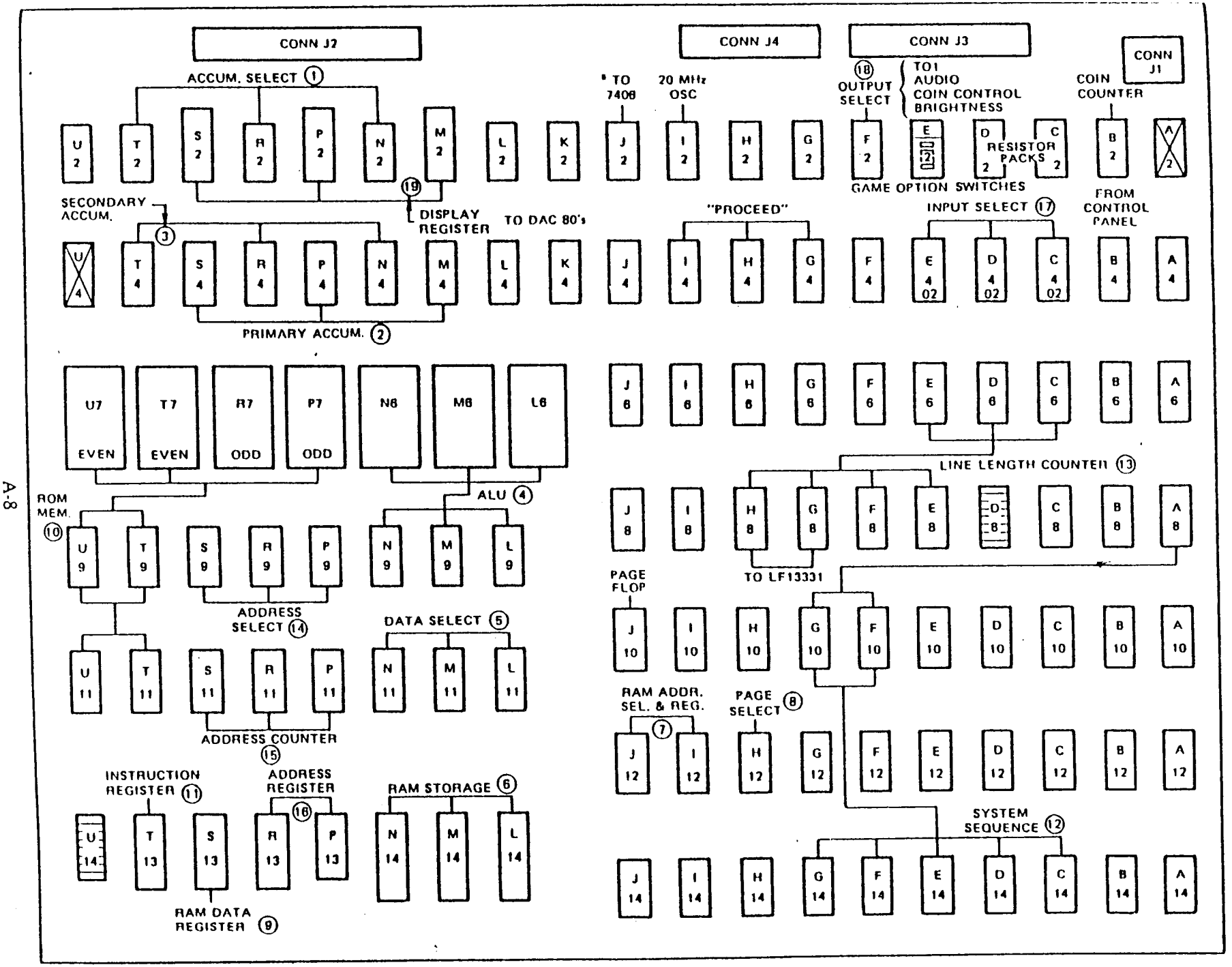
CHIP LOC.	J3	INPUT	SW	SH	SD	TG	RO	SC
	1	X	X	X	X	X	X	X
	2	Vcc.+5	X	X	Vcc.	Vcc.	X	X
E4-4	3	SO	Right Fire	1 Player Select	Opt. Sw.	Opt. Sw.	Opt. Sw.	Opt. Sw.
E4 - 1	4	S3	Right Hyp	#1 Fire	Sw.	Sw.	Sw.	Sw.
E4 - 2	5	S2	Left Fire	Sel. 2	X	Sw.	Sw.	Sw.
E4 - 3	6	S1	Left Hyper	#2 Fire	X	Sw.	Sw.	Sw.
E4 - 13	7	S6	Reset	X	X	Sw.	Sw.	Sw.
D4 - 1	8	P3	9	#1 Dwn	2 Player	X	Start 2	X
D4 - 2	9	P2	4	#1 Right	1 Player	X	#2 Right	2 Start
D4 - 3	10	P1	8	#1 Left	Left Fire	X	Start 1	X
D4 - 4	11	P0	3	#1 UP	LBIT 0	X	#2 Left	1 Start
D4 - 12	12	P7	7	X	Right Fire	Start	X	X
D4 - 13	13	P6	2	X	4 Suns	Shield	X	Left
D4 - 14	14	P5	6	#2 Dwn	Grid	Fire	#2 Fire	X
D4 - 15	15	P4	1	#2 Right	3 Suns	X	#2 Forward	X
C4 - 1	16	P11	0	#2 Up	2 Suns	X	X	X
C4 - 2	17	P10	5	#2 Left	RBIT 0	X	X	Fwd.
C4 - 3	18	P9	Right Fwd	#1 Fast	LBIT 1	X	X	X
C4 - 4	19	P8	L Left	#2 Slow	RBIT 1	X	X	Right
C4 - 15	20	P12	R Right	#1 Med	LBIT 2	X	#1 Left	Fire
C4 - 14	21	P13	L Right	#2 Med	RBIT 2	X	#1 Fire	X
C4 - 13	22	P14	R Left	#1 Slow	LBIT 3	X	#1Right	X
C4 - 12	23	P15	L Fwd	#2 Fast	RBIT 3	X	#1 Fwd	X
	24	N/C	Coin	Coin	Coin	Coin	Coin	Coin
	25	N/O	Coin	Coin	Coin	Coin	Coin	Coin
	26	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd

SCHEMATICS and

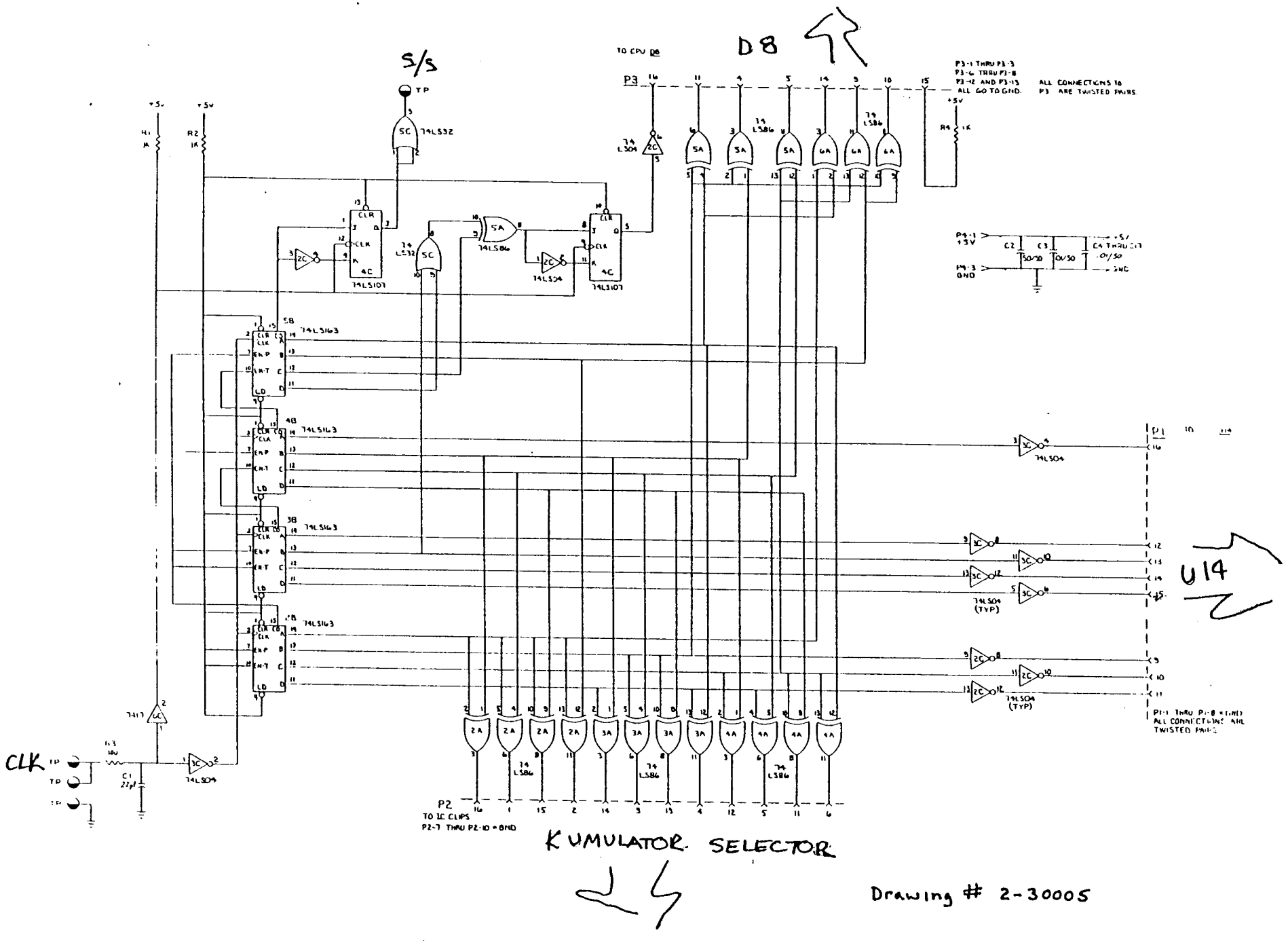
ASSEMBLY DRAWINGS

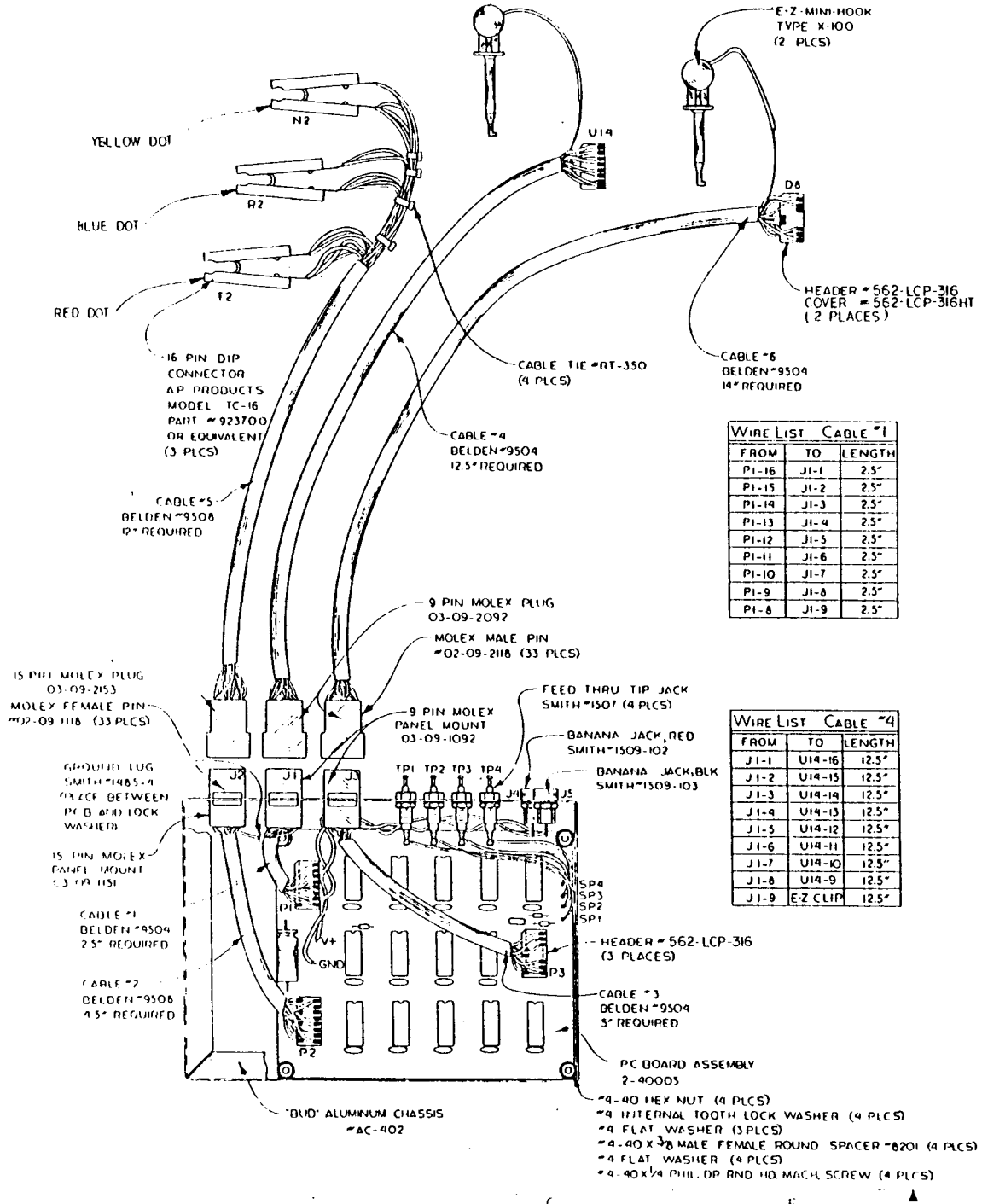


Drawing # 2-40005



*OR 16-LEVEL INTENSITY CIRCUITRY


S/S
TO CPU D0
D8
P3
P3-1 THRU P3-3
P3-6 THRU P3-8
P3-12 AND P3-13
ALL GO TO GND.
ALL CONNECTIONS TO P3 ARE TWISTED PAIRS.
+5V
TP
74LS32
74LS04
74LS86
74LS107
74LS163
5B
4B
3B
2B
74LS04 (TYP)
U14
P1
P1-1 THRU P1-8 = GND
ALL CONNECTIONS ARE TWISTED PAIRS
CLK
C1 22pF
P2
TO IC CLIPS
P2-1 THRU P2-10 = GND
KUMULATOR SELECTOR
Drawing # 2-30005



WIRE LIST		
FROM	TO	LENGTH
SP1	TP1	4"
SP2	TP2	3.5"
SP3	TP3	3"
SP4	TP4	2.5"
V+	J4	7.5"
GND	J5	7.5"

} TWISTED PAIR 22 GA

WIRE LIST CABLE #1		
FROM	TO	LENGTH
P1-16	J1-1	2.5"
P1-15	J1-2	2.5"
P1-14	J1-3	2.5"
P1-13	J1-4	2.5"
P1-12	J1-5	2.5"
P1-11	J1-6	2.5"
P1-10	J1-7	2.5"
P1-9	J1-8	2.5"
P1-8	J1-9	2.5"

WIRE LIST CABLE #3		
FROM	TO	LENGTH
P3-4	J3-1	5"
P3-5	J3-2	5"
P3-6	J3-3	5"
P3-9	J3-4	5"
P3-10	J3-5	5"
P3-11	J3-6	5"
P3-14	J3-7	5"
P3-15	J3-8	5"
P3-16	J3-9	5"

WIRE LIST CABLE #5		
FROM	TO	LENGTH
J2-1	N2-9	12"
J2-2	N2-4	12"
J2-3	R2-9	11.5"
J2-4	R2-4	11"
J2-5	T2-9	10"
J2-6	T2-4	10"
J2-7	R2-8	11"
J2-8	T2-8	11"
J2-9	N2-8	12"
J2-10	T2-7	10"
J2-11	T2-12	10"
J2-12	R2-7	11"
J2-14	R2-12	11.5"
J2-15	N2-7	12"
J2-13	N2-12	12"

WIRE LIST CABLE #4		
FROM	TO	LENGTH
J1-1	U19-16	12.5"
J1-2	U19-15	12.5"
J1-3	U19-14	12.5"
J1-4	U19-13	12.5"
J1-5	U19-12	12.5"
J1-6	U19-11	12.5"
J1-7	U19-10	12.5"
J1-8	U19-9	12.5"
J1-9	E-Z CLIP	12.5"

WIRE LIST CABLE #6		
FROM	TO	LENGTH
J3-1	D8-4	14"
J3-2	D8-5	14"
J3-3	E-Z CLIP	14"
J3-4	D8-9	14"
J3-5	D8-10	14"
J3-6	D8-11	14"
J3-7	D8-14	14"
J3-8	D8-15	14"
J3-9	D8-16	14"

WIRE LIST CABLE #2		
FROM	TO	LENGTH
P2-1	J2-1	4.5"
P2-2	J2-2	4.5"
P2-3	J2-3	4.5"
P2-4	J2-4	4.5"
P2-5	J2-5	4.5"
P2-6	J2-6	4.5"
P2-7	J2-7	4.5"
P2-8	J2-8	4.5"
P2-9	J2-9	4.5"
P2-10	GND LUG	4.5"
P2-11	J2-10	4.5"
P2-12	J2-11	4.5"
P2-13	J2-12	4.5"
P2-14	J2-14	4.5"
P2-15	J2-15	4.5"
P2-16	J2-13	4.5"

Drawing # AD100400

VECTORBEAM™ MONITORS: DEMYSTIFIED

Finally, all you've ever wanted to know about vector displays but were afraid to ask! After reading this article your sex life will improve, your car will never fail again, the price of gasoline will go down and the hostages will be released. Take it from some guy just like yourself who once couldn't pour water out of a pail with the directions on the bottom:

"I see the light. Now get that match out of my face."
-Don Wright, Customer Service Engineer

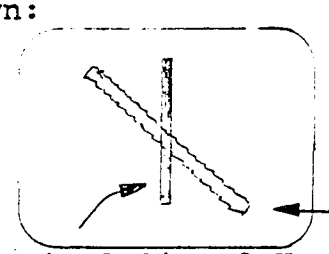
VECTOR THEORY

VECTOR VS RASTER

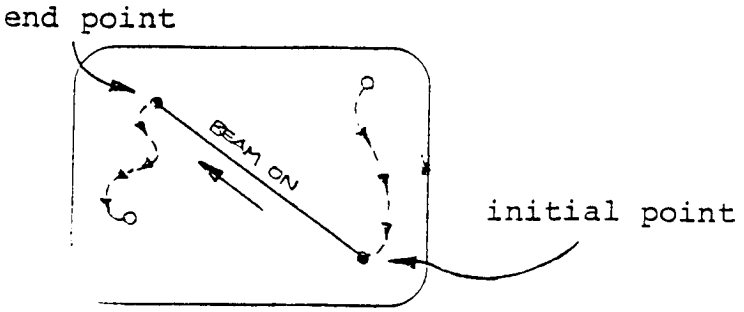
On a typical, old fashioned raster system, the beam is constantly scanned horizontally across the face of the CRT as shown below. It takes about 525 sweeps for the beam to cover the entire picture; but only 425 lines comprise the actual viewfield. In order to draw a character on the raster display, the beam is turned on at the right

Old Fashioned Raster Scan System

point in the scan pattern, and turned off otherwise. Hence all images are displayed in horizontal "slices". The drawback is that slanted lines appear non-uniform and ragged due to this "slice" display technique, as shown:



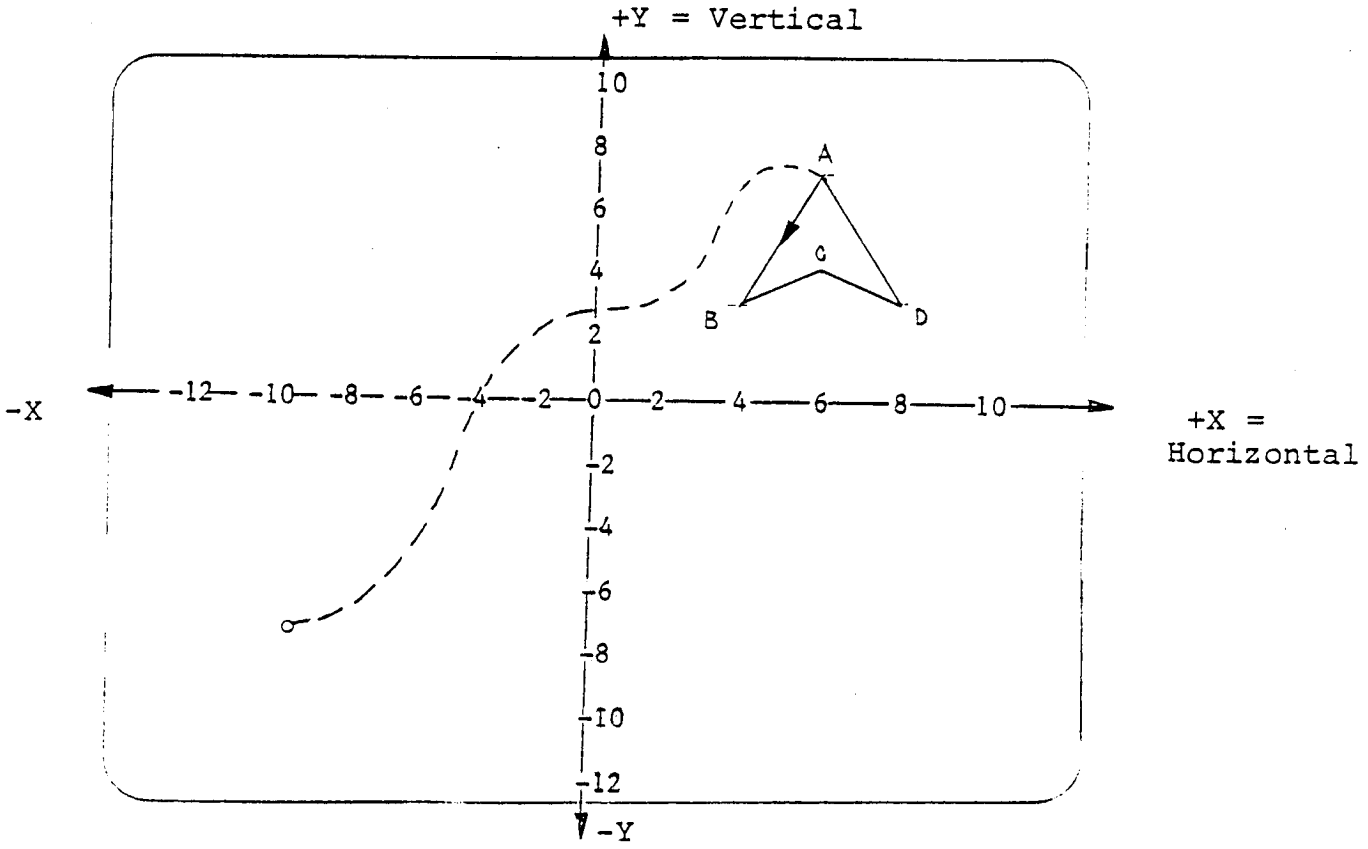
On an exciting vector display, lines drawn at even smaller angles are perfect and exact. The resolution and detail possible is equivalent to that found on a good oscilloscope, and, as a matter of fact, the operation of both are identical when the scope is used in the X-Y mode! This is because when a line is drawn on a vector system, the beam is initialized at one end of the line, turned on, and deflected smoothly to the end point of the line resulting in a perfectly smooth, scope quality vector. Whom would you want to associate with: a raster man or a vectorbeam man?



VECTOR MATH

A vector system is so named because all the characters are made of straight lines termed "vectors" in math-talk. A vector is simply a line that has an initial starting point and a final end point. If the face of the picture tube is divided into so many horizontal counts and so many vertical counts, the end points of a vector can be found by starting in the center and going so many counts horizontal and so many counts vertical. A piece of cake, eh?

Lets divide the screen into horizontal and vertical counts as shown below:

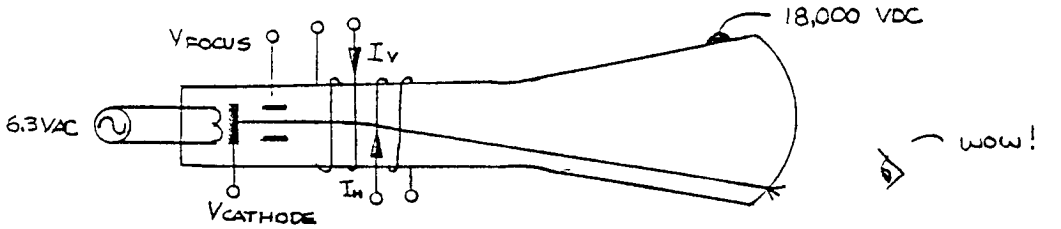


In order to draw the ship, we need to specify the initial point of the vector segment AB. To get to point A from the origin, we need to go 6 counts positive horizontally and 7 counts positive vertically. Point A therefore has coordinates (6,7). Similiarly, B has coordinates (4,3). If the beam was screwing off somewhere else in the picture, feeding the deflection section of the monitor the initial point A coordinates (6,7) would cause the beam to fly to that point.

Next we simply turn the beam on and feed in endpoints (4,3) and the beam proceeds to that point. To complete the picture, we just specify the coordinates for C & D. Now wasn't that easy!

THE BEGINNING

Some smart guy discovered that a magnet placed close to a beam of electrons caused the beam to bend or deflect slightly off a straight course. The stronger the magnet, the more the deflection. From this he decided to take a beam of electrons, a coil of wire and some electronics to provide a variable current source and make a device for playing games. The figure below illustrates the device he came up with:

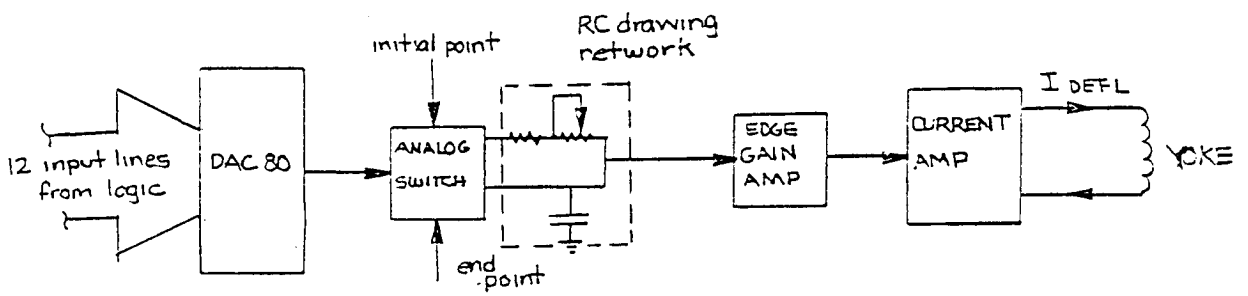


The filament heats up a piece of metal called the cathode. This excites the electrons which are attracted by the 18KV potential at the face (anode) of the CRT. What we actually see is the energy released from the electrons when they strike the phosphors at the tube face. Current entering the horizontal and vertical deflection coils can position the beam at any coordinate point on the face of the tube. A focus voltage narrows the beam into a fine diameter.

MONITOR THEORY & TEST PROCEDURE

The ciruits on the vector monitor can be grouped into three catagories, the deflection circuit, high voltage oscillator, and intensity control. The most common failure mode is blowing ± 25 circuit breakers CB1 and CB2. The breakers limit the current going into the yoke to about three amps. To troubleshoot, disconnect the yoke winding, reset breakers, and power up. The breakers should not blow. If they do, the problem is one of the power transistors on the left side panel heat sinks.

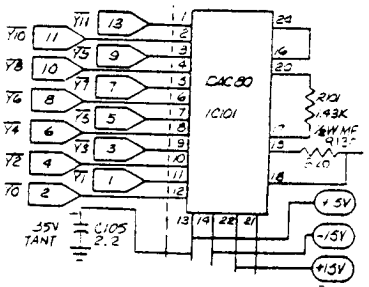
DEFLECTION SECTION



The deflection circuit receives numbers from the logic board in digital form that represent the coordinates for the beginning and end points of each line segment. The output is a current to the yoke windings that is porportional to this number. So the purpose of the deflection circuitry is to convert a binary coded number into a current.

DAC - Digital to Analog Converter

The first step is to convert the digital coordinate number into an analog voltage. The DAC 80 is a device that does this.

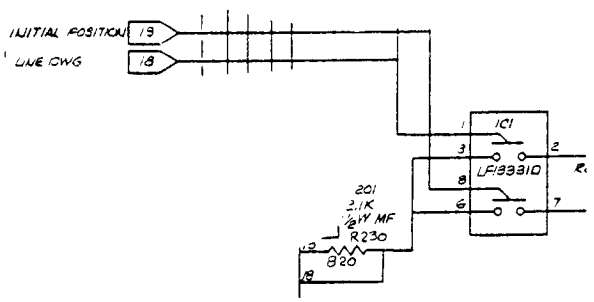


Pins 1 thru 12 can represent any number between -2048 and +2047. The output voltage range is from -5 volts to +5 volts. When a DAC is operating properly, the output signal is centered about 0 volts and bounded between ±5 volts.

TEST PROCEDURE

Verify proper power on pins 13, 14, and 22. A DC meter should read approximately 0 volts at pin 15. Check pins 1 thru 12 with a logic probe; most of the lines should be pulsed.

ANALOG SWITCH - LF13331



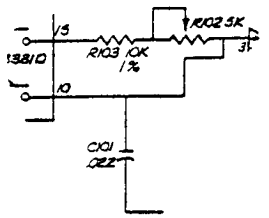
The analog switch is the most active component on the monitor. Both horizontal and vertical DAC output voltages pass through this switch and then become converted into currents to deflect the beam to proper positions on the screen. It is mounted in a socket for easy removal and should be a prime suspect for a monitor that blows circuit breakers.

The switch passes the voltage output of the DACs through either of two channels: the lower channel is for the initial position coordinate of a line segment, and the upper channel for the final coordinate. The channels are controlled by the CPU: initial position on pin 8 and line drawing (final coordinate) on pin 1. If the upper channel in the switch is defective, say, in the vertical section, then there will be no vertical lines on the display. The same is true for the horizontal.

TEST PROCEDURE

Thereshould be a charging waveform centered about 0 volts on the switch output pins. The upper channel waveform should be of greater peak to peak magnitude than the lower channel. Replace the switch.

RC VECTOR DRAWING NETWORK



The RC network is responsible for drawing smooth, straight and precisely positioned vectors. It combines together the two channels of the analog switch in the manner necessary to draw the vertical and horizontal line segments.

Initial position voltages enter from the lower switch channel directly across C101, which charges to that level extremely rapidly. This voltage is converted to an initial position current that positions the beam at the beginning point of a line segment.

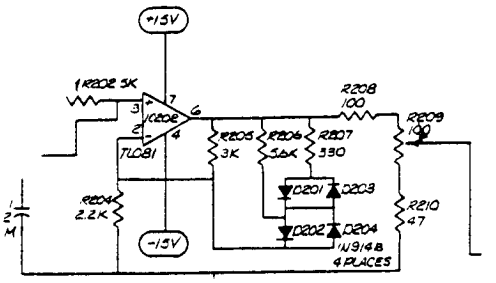
Final position data from the upper switch channel slowly charges C101 through R103 and line length pot R102. As C101 charges from its initial point value to its final value, a straight vector is drawn. It's as simple as that!

Pot R102 varies the charge rate of the network, and can lenghten (faster charge) or shorten (slower charge) the vector for the "on" period of the beam.

TEST PROCEDURE

If line segments are adjustable but bowed, replace C101. If line segments cannot be adjusted to intersect, verify proper resistance of R103 and R102 as R102 is rotated.

EDGE GAIN AMPLIFIER



The edge gain amplifier is the final stage before the voltage to current conversion process. The input on pin 3 is a waveform that is the composite of initial position and final position data signals. The amplifier has an overall gain of about two at output pin 6. The waveform should resemble the DAC output but is bounded between ±2 volts, centered about 0 volts.

It is a property of the CRT that, near the edges, the amount of current needed to move the beam, say, an inch, is less than the amount required to deflect the beam an inch off the center. Therefore, less gain is required near the edges of the CRT.

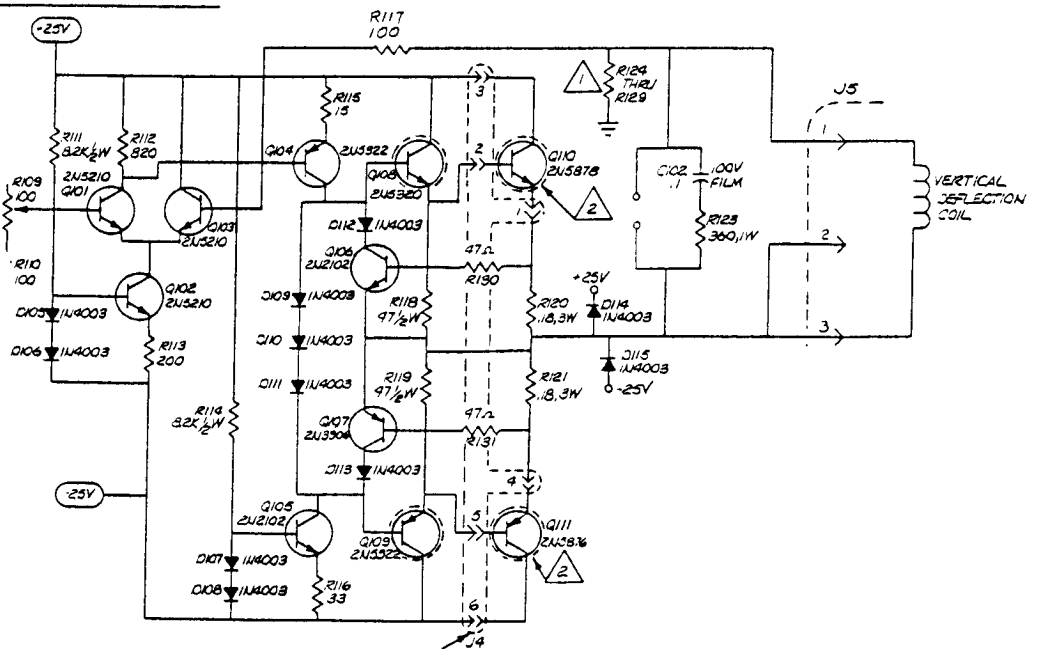
The amplifier circuit reduces gain as the output voltage increases, indicating a larger beam displacement, by switching on diodes D201 and D202 for the left half of the screen, and D203 and D204 for the right half. This places R206 and R207 in parallel with R205, reducing its value and consequently the gain. If a figure increases in size near the display edges a diode is open.

R209 is the horizontal picture size control. By picking off larger or smaller voltages, the width of the picture is controlled.

TEST PROCEDURE

Observe signal at pin 3. Waveform to pin 6 should be the same with an average gain of two. Signal should be centered and bounded between ±2 volts. Check D201 - D204.

DEFLECTION AMPLIFIER



The deflection amplifier converts the pick off voltages from the size pot into a current to drive the yoke winding. The input is a differential stage consisting of transistors Q101, Q103, and Q102. Q102 is a constant current source and a fixed amount of current always flows through it. If this current varies, the picture will be offset from center. Too much offset will cause circuit breakers to blow.

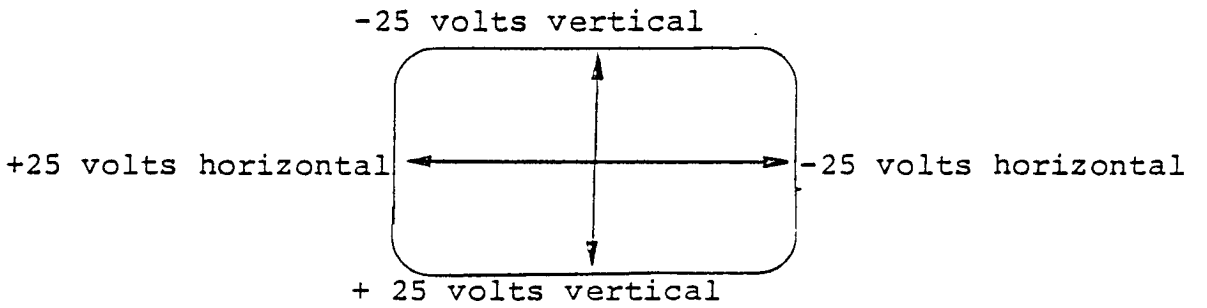
This reference current is determined by the voltage drop across R113. Diodes D105 and D106 determine this drop. The voltage across one of the diodes is cancelled by the base-emitter voltage of Q102. R113 should constantly read .6 volts DC. This means a constant flow of about 3ma through Q102.

This 3ma bias must come from the emitters of Q102 and Q103. Excess current is picked off at the collector of Q101 and feeds pre-driver Q104. The constant current source for pre-driver Q104 is Q105, D107, D108, and R116. Bias current through R116 is about 22ma

Current is delivered to the yoke in a push-pull manner by transistor pairs Q108 and Q110 for positive current transitions and Q109 and Q111 for negative current transitions. Q110 and Q111 are power drivers mounted on humongous heatsinks on the left side panels.

Diodes D109, 110, and 111 set up a crossover voltage threshold to prevent both halves of the push-pull output form turning on at the same time. Should one of the diodes open, only half of a display will be generated. Should they become resistive, both power transistors will turn on simultaneously and generate excessive heat.

If more than three amps are drawn through sense resistors R120 and 121, transistors Q106 and Q107 turn on and shut off the power driver by sinking the base current to drivers Q108 and Q109. This protects the hardware against further damage.



Voltage wise, the CRT is bounded according to the above drawing. If there is a problem with the upper half of the picture, it is with the circuit elements connected to the -25 volt line in the deflection amplifier. If, say, the last half of the picture is missing, suspect the elements connected to the +25 volt side of the horizontal amplifier.

TEST PROCEDURE

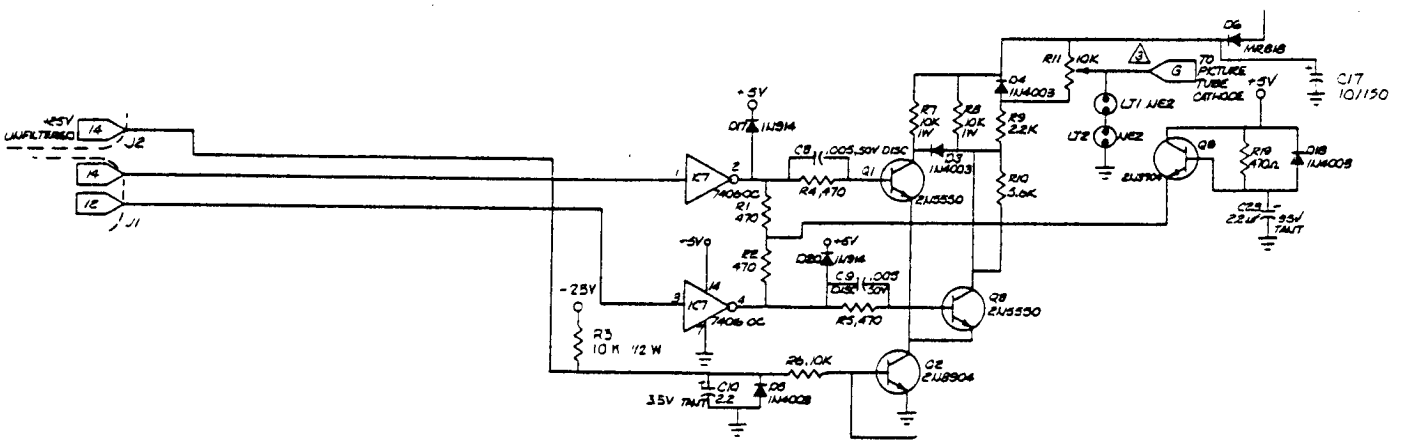
If the game is blowing circuit breakers the problem nine times out of ten is a transistor in the deflection section. Recommended procedure is to check each transistor in circuit with a transistor checker. Lift diodes D112 and D113 to check transistors Q106 and Q107. D212 and D213 in the horizontal section.

If a scope is available, the defective chanels can easily be located. Step one: remove yoke connector from display board. Step two: Reset breakers and power up game. With scope, probe the cases of transistors Q104 and Q204. There should be pulses clipped at ±25 volts. The defective channel will not have these.

Replace the analog switch IC1. This is the quickest manner to verify proper operation.

Once the channel is located, start at the DAC's and proceed forward according to the aforementioned theory.

INTENSITY CIRCUIT



The beam can be turned on and off by applying the proper voltage level to the CRT cathode. Beam cut off is +90 volts D C. At this potential, the electrons excited by the filament prefer to remain on the cathode and none make it to the CRT. Lowering this potential allows more electrons to escape to the anode. We can then produce a Normal Intensity level by lowering the cathode potential to 40VDC and a Hi Intensity by lowering the potential to, say, 20VDC.

The computer produces two intensity levels by sending low pulses to pins 1 and 3 of IC 7. Pin 1 is the HI INTENSITY channel and consists of IC7 and Q1. The NORMAL INTENSITY channel consists of another part of IC7 and Q3.

A beam blanking voltage of +90 VDC is generated from pin 8 of the H.V.XFMR secondary winding, D6 and C17. This half wave rectifier supplies this +90 volts to one terminal of the brightness pot. The wiper of this pot picks off the proper voltage and sends it through the yellow cathode wire to the CRT plug socket.

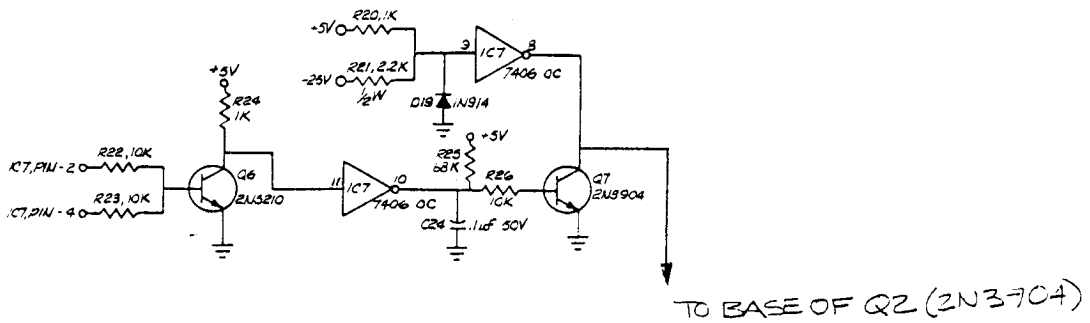
With Q1 and Q3 both off, current has no path to ground and the wiper voltage will be +90 volts regardless of the brightness pot setting. For a NORMAL INTENSITY vector, pin 3 of IC7 pulses low. Pin 4 then pulses high to 2.75 volts, turning on Q3. Current flows through R11, R9, R10 and through Q3 to ground via Q2. This drops the voltage at the cathode to about +40 volts with the brightness pot full clockwise.

For a HI INTENSITY vector, pin 1 of IC7 pulses low. Output pin 2 pulses high to 2.75 volts, turning on Q1. Current flows through R11, R9, through Q1 and to ground via Q2. This drops the cathode level to 20 volts with the brightness pot full clockwise.

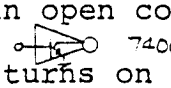
The yellow wire to the cathode should show a 90 volt DC base with negative going pulses that vary as the brightness pot is turned. For a no display condition, suspect IC7(7406). This chip is an open collector inverter and must have a pull-up resistor on its output. Verify that 4-5 volts is always present at the junction of R1 and R2. This voltage is supplied by Q8, which is in an RC delay circuit to allow all voltages to settle on power up before a picture is displayed.

Q2 is designed to open the intensity circuit immediately after power is removed from the game. This prevents the +90 volt blanking voltage from bleeding off before the high voltage bleeds off, thus preventing a spot when the game is unplugged. Q2 is kept on continually by a full wave rectified, unfiltered signal from the power supply through fuse F1(0.5A). For a no display condition eliminate Q2 as a source of trouble by jumpering it collector to emitter.

PROTECTION CIRCUITRY



Q2 can be considered as the master intensity control switch. When it is deprived of its base drive, the collector-emitter junction opens and eliminates the ground path for the intensity channels, cutting off the beam. The logic board can fail in such a way as to cause the beam to remain on continuously, burning the CRT phospher.

R25 and C24 form a RC time constant of about 6.8ms. Since most of the vectors on the display require only microseconds of beam time, any turn on pulse from the CPU 6.8ms or wider constitutes a failure mode. The outputs of IC7-2,4 are sampled by Q6, which inverts the pulses and feeds them to IC7 pin 11. IC7 is an open collector inverter and its output stage looks as follows:  7406
When the input is high, the output transistor turns on and essentially shorts pin 10 to ground. When the input is low, the transistor turns off and opens the circuits. So, for example, a high pulse at IC7-4 of 10ms duration becomes a low pulse at the collector of Q6. This causes IC7 pin 10 to open the circuit, allowing C24 to charge. Since the pulse width is greater than 6.8ms, C24 has ample time to charge and turns on Q7, which shorts the base of the master intensity switch Q2, killing the display.

Another protection circuit involves R20, R21 and pins 9 and 8 of IC7. Pin 9 is normally held negative by the voltage divider of R20 and R21. Should the circuit breakers blow and we lose -25 volts, pin 9 goes positive causing pin 8 to short the base of Q2, again killing the display.

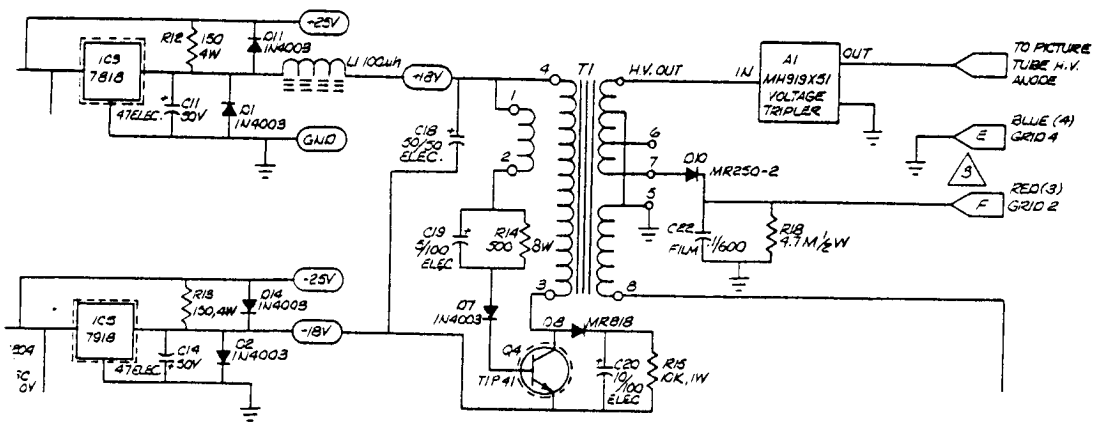
TEST PROCEDURES

To isolate a no display condition to the intensity circuit, probe the yellow cathode wire at the CRT plug, turn the brightness full clockwise and observe a +90 volt base with pulses at 40 volts. If pulses are missing, jumper Q2 collector to emitter. If picture returns, check F1 in power supply. Replace Q2.

Observe 2.75 volt pulses at pin 4 of IC7. If missing, verify pulses at input pin 3. Check for +5 volts at junction of R1 and R2. Replace IC7.

If pulses are at +4 volts, replace Q2. The output of pin 4 will exceed 2.75 volts if there is no load due to a failed transistor.

HIGH VOLTAGE OSCILLATOR



The integral elements of the HV oscillator section are IC9, IC5, Q4 and flyback XFMR T1. The ±18 volt regulators IC9 and IC5 deliver 36 volts across C18. The frequency of oscillation is dependent on the winding characteristics of HV XFMR T1. As current begins to flow through pin 4, a reverse potential is induced in the tickler coil at pins 1 and 2, tending to shut off Q4. Q4 turns on again after the R14/C19 time constant discharges, repeating the cycle. The tank circuit of D8, R15 and C20 provide a protective sink circuit against inductive spikes that must otherwise cripple the TIP41C. Diode D7 protects against reverse currents.

The secondary windings generate an 800 volt p-p vaveform at pin 7 that is half wave rectified by D10 and filtered by C22 to provide +400 volts DC of focus control.

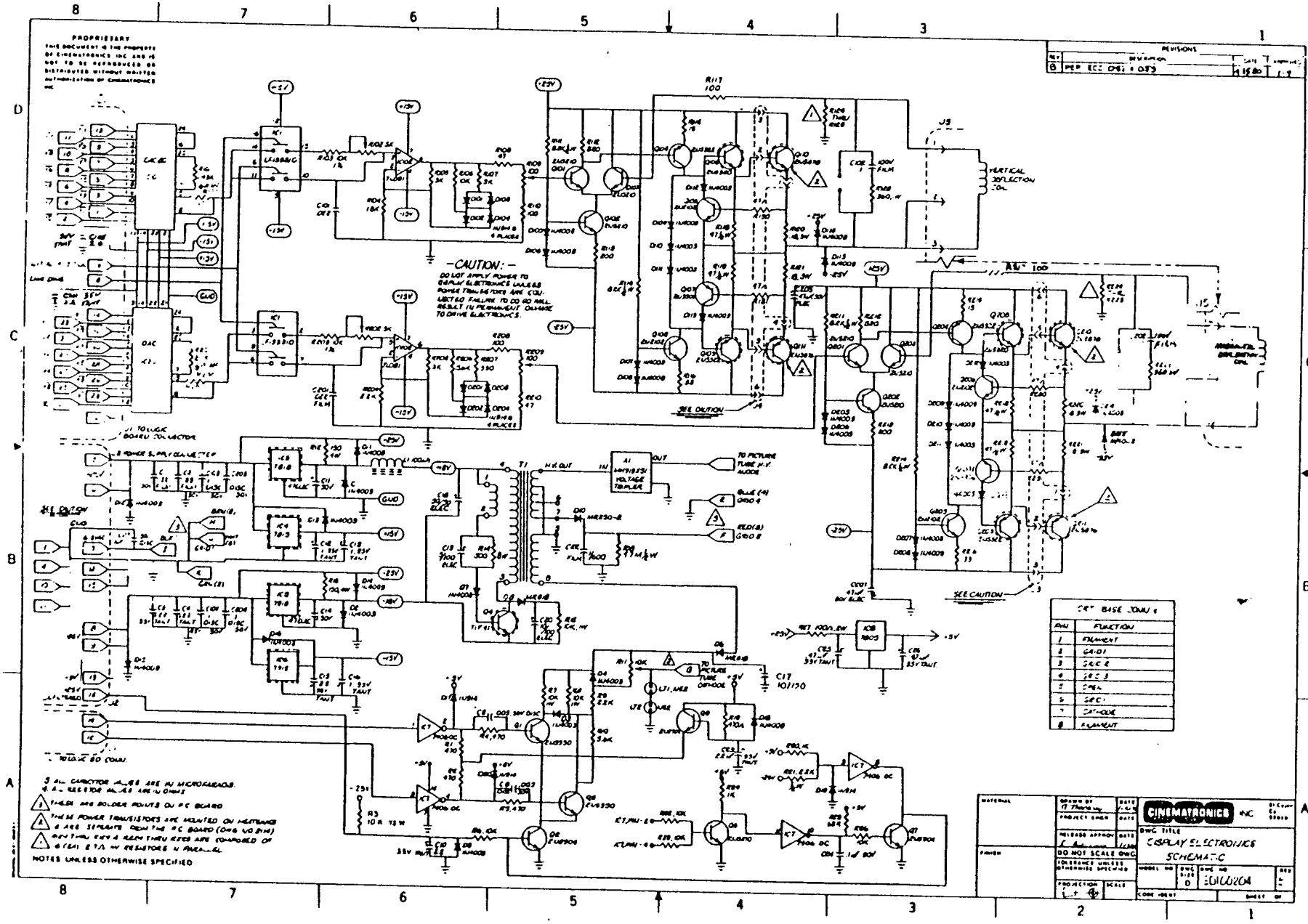
Beam cutoff voltages (+90 VDC) is supplied by a 200 volt p-p signal on pin 8, rectified by D6 and filtered by C17.

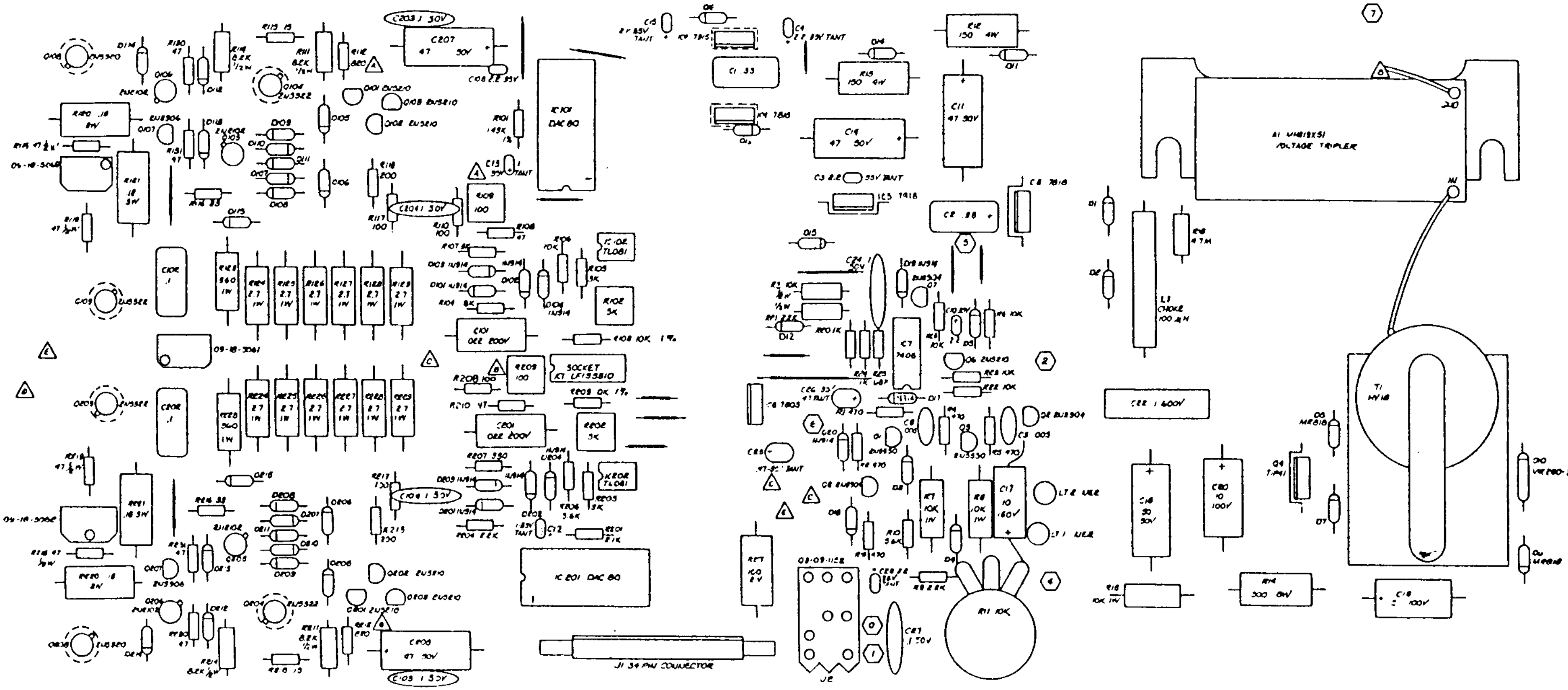
TEST PROCEDURES

The vast majority of HV failures will be the TIP41C. When this component fails, it will cause the +18 volt regulator to shut down internally due to a now excessive load request, say, if Q4 shorted. Remove pin 3 of the transformer winding. With the load removed, the +18 volt regulator should read +18 volts. The -18 volt regulator will read -18 or -25 volts. Replace Q4, C17, D7 and the defective regulator all at once.

D10 and D6 are high voltage, fast recovery diodes that will not read with an ordinary meter. To test, lift cathode from circuit and observe rectifying properties.

Congratulations! This is the end. You made it.


PROPRIETARY
REVISIONS
-CAUTION:-
DO NOT APPLY POWER TO DISPLAY ELECTRONICS UNLESS POWER TRANSISTORS ARE COOL. HEAT FAILURE TO DO SO WILL RESULT IN PERMANENT DAMAGE TO DRIVE ELECTRONICS.
CRT BASE DIAGRAM
PIN FUNCTION
1 FILAMENT
2 GRID 1
3 GRID 2
4 GRID 3
5 SPARE
6 GRID 1
7 CATHODE
8 FILAMENT
CINEMATRONICS INC
DWG TITLE
DISPLAY ELECTRONICS SCHEMATIC
DO NOT SCALE DWG
SCHEMATIC



A = #22 BROWN 2"
B = #22 BROWN 3½" (TRU)
C = #18 BLACK 4¾"
D = #18 RED 3"
E = #18 BLUE 3"

0 BLACK 3½"
1 BROWN 10½" — TWIST TOGETHER
2 RED 2"
4 YELLOW 10"
5 GREEN 3"
6 BLUE 11½"
7 WHITE 13"

3 ALL DIODES ARE IN4003 UNLESS OTHERWISE SPECIFIED.
2 ALL RESISTOR VALUES ARE IN OHM ¼W UNLESS OTHERWISE SPECIFIED
1 ALL CAPACITOR VALUES ARE IN μF

MATERIAL:	DRAWN BY	DATE	CINEMATRONICS INC	
FINISH: BREAK ALL SHARP EDGES AND DEBURR ALL HOLES.	PROJECT ENGR	DATE	DWG TITLE: DISPLAY PCB ASSY	
	RELEASE APPROV	DATE		
	DO NOT SCALE DWG			
	TOLERANCE UNLESS OTHERWISE SPECIFIED		MODEL NO / DWG SIZE / DWG NO: AE 205203	REV: A
	PROJECTION	SCALE: NONE	CODE IDENT	SHEET 1 OF 1

AUDIO BOARDS

Input:

1) Control Circuit

Control lines come from 74LS259 (F2 on logic board.)
The LS7414 is a Schmitt trigger inverter. The 74LS164 is a serial to parallel register and must be enabled by aclock signal at Pin 8 along with data on Pin 1.
The 74LS 377 is a "D" latch. Whatever input is sitting on "D" will be latched to the "D" output with every clock pulse on Pin 11.

2) Noise Generator Circuits

a) The S2688 is a digital random noise generator outputting 12V P-P. (+3V to +15V - on all the time)
b) The 555 is a timer which is controlled by an RC network - outputting 4.4V P-P.
c) The 556 is simply a dual 555 timer.
d) The 566 is an oscillator outputting a 5V P-P square wave.

3) Operational Amplifiers

TL081 op amp or CA3080 (current controlled amp.)

a) The TL081 can be used as a voltage follower, an amplifier or a filter. A signal is introduced either on Pin 2 or 3, inverting and non-inverting respectively. The gain is measured by dividing RF(Feed back resistance) by Resistance in. The main thing to remember is that without a signal applied, there should be no DC offset on Pin 6 of the TL081 and no DC on Pins 2 or 3.

b) The CA3080 is a current controlled amplifier. It works much in the same way that a TL081 does except that it is enabled by a switching transistor. The collector of this transistor, when quiescent will be sitting at -15V. When a signal is applied, the collector will swing in a positive direction thus enabling the CA3080 by injecting a current on Pin 5.

4) Gated Octave Adders (the 74LS393)

This component is utilized in giving a sound a particular pitch. The different outputs which are square waves are beat together giving a definite sound. When only one output of an LS393 is used, then the chip acts as a divider, reducing the frequency, and therefore the pitch.

5) Digital to Analog Conversion

The "D" latch (74LS377) has 3 outputs (Hi's & Lo's) which drive the digital to analog conversion circuitry. the voltages developed on the resistor network are then amplified, filtered and shaped.

6) Output Circuitry

Consists of a pre-amplifier, a final amplifier and power transistors, 3 470pf caps, 2 150 ohm resistors and one 22K ohms resistor.

7) Voltage Regulators

The 7815 has a +25 V input and will output +15V DC.
The 7915 has a -25 V input and will output -15V DC.

Troubleshooting hints for Rip Off and Star Castle

a) Working Back from output circuitry, starting with pre-amplifier, short Pins 2 & 3 of the Op Amp and noise will disappera. In this manner the problem circuit can be isolated.

b) If laser circuit is malfunctioning, suspect 7406 or 74LS393 (or 74LS259 (F2) on the logic board).

c) If background sound is not correct in pitch or frequency, suspect 74LS393.

d) For constant high frequency noise, suspect input control 74LS377, ("D" latch 74LS164 (S/P register) or 7414 (Schmitt-trigger inverter).

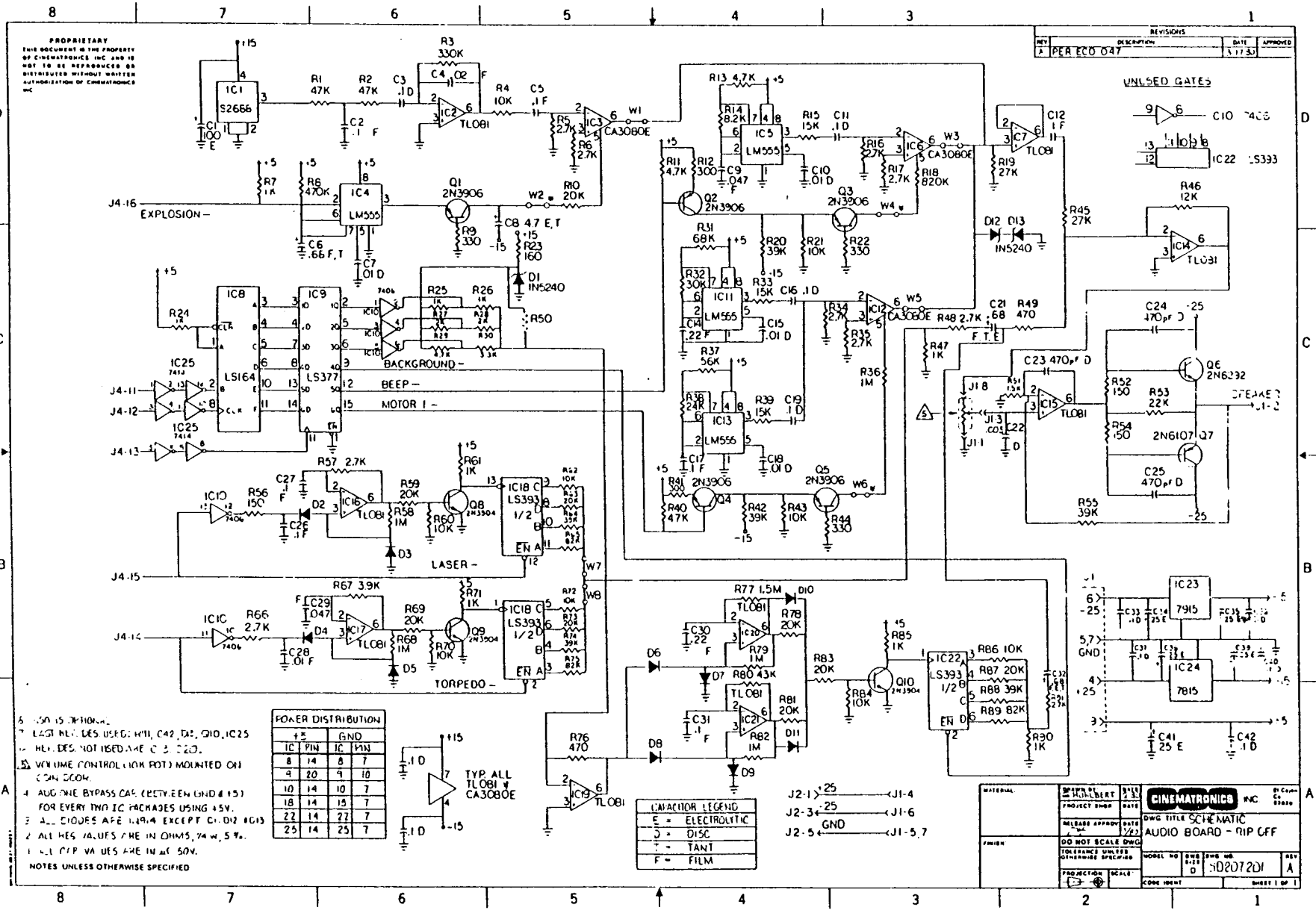
e) For constant or missing loud or soft explosion, torpedo or laser suspect 74LS259 position F2 on logic board or noise generator of particular circuit.

f) No sound, but signal clicks in speaker, suspect noise generator circuitry.

g) Faulty 7915 regulator. Check input at -25V if 7915 is not outputting -15V, lift trace at output. If -15V not there replace 7915. If -15V is there, repair trace and lift leg of each component being fed by -15 V. When -15V comes up, replace component holing 7915 down.
If 7915 is bad check for DC level on Pin 6 of final amplifier. If DC is present with no DC offset on Pins 2 or 3 on Op Amp, replace TL081 and final output circuit.

h) Troubleshooting Final Output Circuit

No suond at all means a blown speaker. Replace speaker, but not before replacing both power transistors 2N6292 and 2N6107. Ohm out both 150 ohms resistors and the 3 470 pf caps in the final output and replace final Op Amp TL081. Make sure no DC offset is present on emitters of 2N6292 or 2N6107. Collector of 2N6292 must have +25V while collector of 2N6107 must have -25V.


PROPRIETARY
REVISIONS
PER ECO 047
UNUSED GATES
EXPLOSION –
BACKGROUND –
BEEP –
MOTOR 1 –
LASER –
TORPEDO –
POWER DISTRIBUTION
CAPACITOR LEGEND
TYP. ALL TL081 & CA3080E
J2-1 .25 J1-4
J2-3 .25 J1-6
J2-5 GND J1-5,7
CINEMATRONICS INC
DWG TITLE SCHEMATIC
AUDIO BOARD - RIP OFF
DO NOT SCALE DWG
SD020720 01
NOTES UNLESS OTHERWISE SPECIFIED